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LOW POWER CHANNEL SELECTION FILTERING FOR HIGHLY INTEGRATED WIRELESS RECEIVERS

PhD. dissertation prepared to obtain the Doctor degree

By

Coro García Alberdi

Supervisor:

Prof. Antonio J. López Martín

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Autor: D.ª Coro García Alberdi

Directores: Prof. Antonio J. López Martín

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A mi familia y amigos

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ABSTRACT

In this research work, low-voltage and low-power techniques have been applied to implement novel analog circuits, mainly Gm-C filters. The structure of the thesis follows a bottom-up scheme: basic techniques at device level are proposed in the first place, followed by the introduction of novel circuit topologies at cell level, and finally the achievement of new designs at system level.

At device level the main contribution of this work is the employment of Floating-Gate (FG) and Quasi-Floating-Gate (QFG) transistors in order to reduce the power consumption. By using them, new topologies are proposed at cell level, being a high-performance tunable class AB transconductor well adapted to low power and low voltage environments the most important one. This circuit employs a resistive divider implemented by MOS transistors operating in triode region as tuning scheme.

Regarding system level, new designs have been achieved by employing these novel cells. In fact, as a final result, this dissertation introduces a new tunable highly-linear third-order Butterworth low-pass Gm-C filter, suitable for channel selection filtering in a Zero-IF receiver. Automatic tuning systems are also proposed to improve it. Moreover, a VGA is also implemented by employing the same basic cell. It operates with constant bandwidth for all the gain settings. Both are important blocks in a Zero-IF wireless receiver.

All the proposed circuits have been fabricated using a 0.5µm double-poly n-well CMOS technology, and the corresponding measurement results are provided and analyzed to validate their operation. Furthermore, different approaches to obtain the final designs are discussed together with theoretical analysis to fully explore the potential of the resulting circuits and systems in the scenario of low-power low-voltage applications.

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RESUMEN

En este trabajo de investigación, se han propuesto y aplicado nuevas técnicas de baja tensión y bajo consumo en diseño analógico para implementar varios circuitos, principalmente filtros Gm-C. La tesis está estructurada en niveles ordenados de abajo hacia arriba: técnicas básicas a nivel de dispositivo se proponen en primer lugar, seguidas por la introducción de nuevas topologías de circuitos a nivel de celda, y finalmente por la obtención de nuevos diseños a nivel de sistema.

A nivel de dispositivo, la mayor contribución de este trabajo es el empleo de transistores de puerta flotante (FG: Floating-Gate) y puerta cuasi-flotante (QFG: Quasi-Floating Gate), cuyo objetivo es la reducción del consumo de potencia. Mediante su empleo se han propuesto nuevas topologías a nivel de circuito, siendo un transconductor sintonizable clase AB adaptado a los requisitos de baja tensión y bajo consumo de los sistemas de comunicaciones modernos la más importante de ellas. Este circuito utiliza como esquema de sintonía un divisor resistivo implementado con transistores MOS operando en la región de triodo.

Finalmente, a nivel de sistema, se han conseguido nuevos diseños que utilizan en su implementación los circuitos propuestos. De hecho, como resultado final, se propone un filtro Butterworth Gm- C paso bajo sintonizable de orden 3 aplicable a la selección de canal en un receptor de conversión directa. A fin de mejorarlo, se han propuesto también sistemas de sintonía automática. Además, se ha implementado también un VGA que emplea el mismo circuito básico, y que presenta un ancho de banda constante para todas las ganancias. Ambos son bloques importantes en un receptor inalámbrico de conversión directa.

Todos los circuitos propuestos en esta tesis han sido fabricados usando una tecnología CMOS n-well doble-poly de 0.5µm. Además, los resultados de las medidas experimentales son presentados y analizados en cada caso para validar el funcionamiento del correspondiente diseño. Asimismo, se incluyen explicaciones teóricas y procedimientos de diseño a modo de validación del potencial de los circuitos propuestos en el campo del diseño de baja tensión y bajo consumo.

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LIST OF ACRONYMS

Acronym	Significance
A/D	Analog/Digital
AC	Alternating Current
ACG	Automatic Gain Control
ADSL	Asymmetric Digital Subscriber Line
BJT	Bipolar-Junction Transistor
BW	Bandwidth
CCII	Second-generation Current Conveyor
CMC	Common-Mode-Control
CMFB	Common-Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
D/A	Digital/Analog
DC	Direct Current
DVB	Digital Video Broadcasting
EPROM	Erasable Programmable Read-Only Memory
FGMOS	Floating-Gate Metal-Oxide-Semiconductor
FG	Floating-Gate
FGT	Floating-Gate Transistor
FoM	Figure of Merit
GB	Gain-Bandwidth Product
G_m-C	Transconductor-Capacitor
IF	Intermediate Frequency

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IM3	3rd -order Intermodulation Distortion
LAN	Local Area Network
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect-Transistor
MOSFET-C	MOSFET- Capacitor
nMOS	Negative-Channel Metal-Oxide-Semiconductor
opamp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
pMOS	Positive-Channel Metal-Oxide-Semiconductor
PpP	Power-per-Pole
PSRR-	Negative Power-Supply-Rejection-Ratio
PSRR+	Positive Power-Supply-Rejection-Ratio
QFG	Quasi-Floating-Gate
QFGMOS	Quasi-Floating-Gate Metal-Oxide-Semiconductor
QFGT	Quasi-Floating-Gate Transistor
RSSI	Received Signal Strength Indication
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
UV	Ultraviolet
V-I	Voltage-Intensity
VDSL	Very high bit-rate Digital Subscriber Line
VGA	Variable Gain Amplifier
VLSI	Very-Large-Scale Integration
WiMAX	Worldwide Interoperability for Microwave Access

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PARAMETER GLOSSARY

PARAMETER	SIGNIFICANCE
C_{GB}	Gate-Bulk capacitance
C_{GD}	Gate-Drain capacitance
C_{GS}	Gate-Source capacitance
C_{ox}	Gate Oxide capacitance per unit area
f_c	Cutoff frequency
g_m	MOS transistor transconductance defined as $\partial I_D/\partial V_{GS}$
G_m	Total transconductance of an OTA or transconductor
I_B	Bias current
i_D	MOS transistor drain current
K	1) Current scaling factor
	2)MOS transistor transconductance coefficient
K_B	Boltzmann constant ($1.38 \cdot 10^{-23}$ J/K)
L	Channel length of a MOS transistor
n	Subthreshold slope factor
P_n	Input-referred noise power
q	Electron charge
r	Channel resistance of a triode transistor
Q_0	Initial electric charge
T	Temperature
U_T	Thermal voltage
V_{CM}	Common-mode voltage

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V_{cn}	Bias voltage in an nMOS cascode transistor
V_{cp}	Bias voltage in a pMOS cascode transistor
V_{DD}	Positive supply voltage
V_{SD}, V_{DS}	Source-drain/ Drain-source voltage of a MOS transistor
V_{SG}, V_{GS}	Source-gate/ Gate-source voltage of a MOS transistor
V_{SS}	Negative supply voltage
V_t	Threshold voltage of a MOS transistor
W	Channel width of a MOS transistor
μ_n	Electron mobility parameter

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Chapter 1

Introduction

The aim of this introductory chapter is to present the framework of the thesis. Section 1.1 is focused on the motivations of the thesis, emphasizing the growing importance of low-voltage low-power design applied to analog circuits and, particularly, to channel selection filters. In fact, a review of the most significant low-voltage and low-power analog design techniques is performed in Section 1.1.1, as well as a discussion about the state of the art of the design of Gm-C continuous-time channel selection filters in 1.1.2. General objectives of the thesis are covered in Section 1.2 and, finally, a summary of the structure of the work is provided in Section 1.3.

1.1 Motivation

In the last decades, there has been a growing demand of low-voltage high-integrated electronic devices, which meets the increasing requirements of modern wireless and wireline communication systems powered by batteries. The goal is for these systems to be small and light, as well as achieving long lifetime for their batteries. Hence the reduction of their power consumption becomes a priority.

Furthermore, as the VLSI technology is led by the CMOS processes, the growing density of integration in CMOS technologies is reducing the thickness of the gate oxide of transistors, leading to a reduction of the supply voltage of the

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designs for reliability reasons and to avoid an excess of electric field intensity in the devices [1]. In addition, it increases the driving capability of the transistor. In the 90s the supply voltage evolved from 5V to 3.3V, and even voltages of 1.8V or 1.2 V were employed in 130nm CMOS technologies. In more modern technologies, such as 90nm and 65nm, voltages of 0.9V [2] are used and, according to SIA Roadmap predictions [3], the tendency is for the supply voltage to keep decreasing. Figure 1.1 illustrates how process-parameters have changed over time, by studying 14 different processes, ranging from 3.0μm down to 0.07μm (L_{min}) [4].

For technologies larger than 0.8μm, V_{dd} stays flat and equal to 5V. In smaller technologies, V_{dd} scales roughly linear with minimum feature size following a staircase function. Oxide thickness, T_{ox}, scales down linearly with technology. And finally, threshold voltage, V_{th}, scales more or less like a square root function.

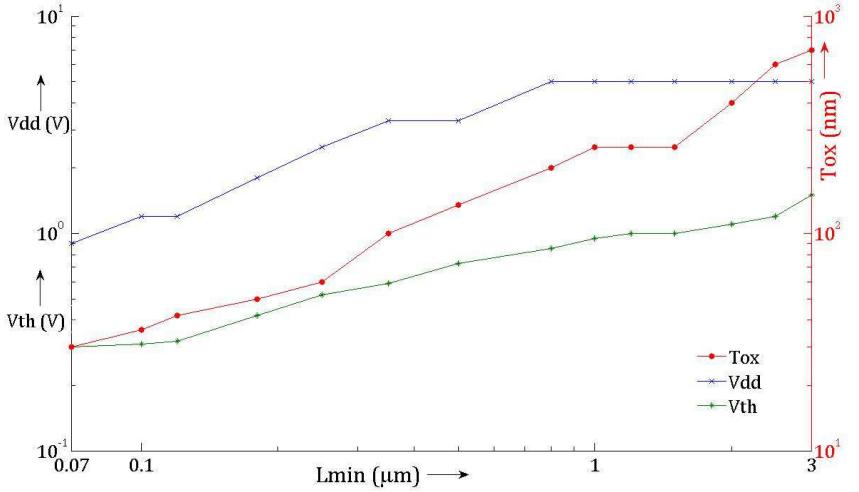

Figure 1.1. Supply Voltage (V_{dd}), Threshold Voltage (V_{th}) and Oxide Thickness (T_{ox}) as a function of Technology geometry (L_{min})[4]

As a consequence of the drastic reduction of the power supplies, they are getting close to the threshold voltages of the MOS transistors, as it is shown in Figure 1.1, and in such a case, digital techniques offer clear benefits with respect to analog ones [5]. Thanks to the way digital signals are processed, CMOS digital circuits have perfectly adapted themselves to these new tendencies. Their level of performance (speed) increases while at the same time the cost (power

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consumption and die area) decreases since they scale with supply voltage. However, issues such as power density and leakage become important. On the other hand, the performance of analog or mixed-signal circuits in newer CMOS generations does not necessarily improve. The most employed solution for combined analog-digital designs, where compatibility between analog and digital blocks is required, has been integrating together on the same chip both analog and digital parts, so that they share the same power supply rail. Thus, the complexity involved in generating various supply voltages can be avoided [6]. However, as opposed to digital case, CMOS analog circuits using conventional techniques suffer from degradation in terms of both dynamic range and signal-to-noise ratio when a reduction of voltage supplies takes place [7], [8]. Therefore, some alternative techniques for analog signal processing are needed.

Furthermore, although digital circuits are easier to design, offer much more robustness and flexibility than analog topologies and its electronic is more versatile in terms of tuning and programmability, there are still some applications where analog electronics is either the most economical and suitable solution or even the only alternative. For instance, interface circuits require a basic analog processing, as physical signals received from the environment are analog and thus have to be minimally treated and adapted for digital processing, and similarly digital signals have to be converted to be delivered back to the analog world.

Under the above conditions, research on new solutions for low supply voltage (twice the threshold voltage of a transistor or even lower) and low power operation is a priority in the design of analog and mixed-signal wireless terminals. Aimed by this need, in this work integrated analog circuits, able to provide innovative solutions for the baseband processing of short-distance wireless receivers, are going to be designed and fabricated. Some applications are aimed to creation of intelligent environments, like a house or a car, wireless connectivity of devices like PCs, or remote medical monitoring. For that reason, their implementation becomes a technological challenge as it combines the necessity of low voltage, low power and high performance.

Among the different blocks that can be employed in analog design following these trends, an important subset is filters. Filters can be useful for many applications in a system such as antialiasing and reconstruction, channel selection or noise reduction. Specifically, among them, this thesis is focused on the application of low-voltage low-power techniques to the design of high-performance continuous-time filters for channel selection, which are a key element of modern wireless and wireline communication systems. Their purpose

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is to discriminate the signal in the desired channel from other undesired signals in adjacent channels, interferences, and out-of-band noise. Large interferers near the desired signal usually demand high linearity, which is often difficult to achieve together with low area and low power consumption.

Traditionally, active-RC filters have been widely employed due to their high linearity (typical THD levels achieved are around -80 dB) [9] and to their high Signal-to-Noise ratio (SNR). However, their main drawback is their limited bandwidth (a few MHz), consequence of the closed-loop operation of the amplifiers. This is due to the classic method followed by active RC topologies for designing stable, linear active circuits by means of feedback using passive linear elements. Another proposal for the design of continuous-time active filters are MOSFET-C filters [10], based on the use of an equivalent CMOS tunable resistor in an RC structure [11], [12]. Similar to traditional active-RC configurations, their use is limited to low-frequency applications due to the requirements of high-performance op-amps. Moreover, their supply voltage is usually constrained by the requirement to tune the active resistors in a wide range.

Current trends in modern communication systems lead to using more elaborated modulation schemes with higher data rates, hence requiring large bandwidth and high linearity for the receiver front-end circuits and analog filters, which makes these classical op-amp based filters unsuitable. For instance, several communication systems like ADSL, VDSL, 802.11a/g/n wireless LANs, WiMax, LTE and DVB use various types of multicarrier modulation schemes. All of them have in common the use of multiple carriers over a wide bandwidth to provide robustness against the impairments of poor quality wireless and wired communication channels. In order to avoid intermodulation distortion among the multiple carriers [13–16], high linearity is required in the entire bandwidth of these systems. For instance, ADSL requires an IM3 better than -60 dB in a signal band of 1.1 MHz, which extends to 4 MHz in ADSL2+, and up to 12 MHz in very high-bit-rate DSL (VDSL) systems [17].

Furthermore, besides these systems that use multicarrier modulation schemes, other systems with other modulation techniques have also special needs that cannot be covered with traditional filter topologies. For instance, the receivers employed in Wireless Personal Area Networks (WPAN). Bluetooth, based on standard IEEE 802.15.1, and Zigbee, based on standard IEEE 802.15.4, are the most popular technologies employed in these systems. Bluetooth is a wireless technology standard for exchanging data over short distances, using short-wavelength radio transmissions in the ISM band from 2400–2480 MHz,

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from fixed and mobile devices, creating personal area networks with high levels of security [18]. It uses a radio technology called frequency-hopping spread spectrum (FHSS), and its latest versions achieve data rates larger than 1Mbps. ZigBee is a low-cost, low-power, wireless mesh network standard. The low cost allows the technology to be widely deployed in wireless control and monitoring applications and the low power-usage allows longer life with smaller batteries [19]. It has a maximum defined rate of 250 kbps and uses also the ISM 2.4 GHz band as well as the 868/915MHz bands. It is mainly used in applications that require a low data rate, long battery life, and secure networking. It employs direct-sequence spread spectrum (DSSS) coding. Although the modulation techniques of these standards require less bandwidth and linearity than those of the multicarrier systems, these requirements must be obtained in this case with much lower power levels, making useful again high linearity low consumption approaches.

An up-to-date proposal, more appropriate for all these modern systems, is based on using Gm-C topologies, i.e. filters based on transconductors and capacitors [20–23]. These filters are simple, and feature tuning capability and higher operating frequencies. Due to their open-loop operation, they usually achieve lower power consumption for a given bandwidth, but they also feature less linearity than the other approaches[24], [25]. This limitation can be avoided by coming back to the classic approach, negative feedback and passive resistors, to achieve highly linear circuits while designing the transconductor. Thanks to this, a highly linear voltage to current (V-I) conversion can be achieved. As a consequence, the linearity levels obtained can be compared to those of active-RC filters [26], [27].

Precisely, the implementation of Gm-C channel selection filters is the main topic of this thesis. As it has been said before, in order to be adapted to modern wireless receiver requirements, the resulting circuits need to achieve high-linearity and be implemented by using low-voltage low-power techniques.

1.1.1 Low-Voltage Low-Power Techniques

Since the beginning of the 90s, an intense research in low-voltage and/or low-power circuits has been developed, growing continuously since then. In fact, from the mid-90s, it has been a very current topic in literature, either in books or analog design journals [28–34]. It must be noted that, in spite of being usually joined in titles, Low-voltage and Low-power are terms generally opposed in analog design [8], making indispensable the use of low-power techniques [35] to approach a very low-voltage design.

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There are different viewpoints to study these techniques. Solutions based on novel cells, modification of classical architectures or new methods of signal processing are some of them. A general overview of these techniques applied to analog design is presented in this Section.

Regarding cell design, it is remarkable the very low-voltage current mirror proposed in [36]. Considering op-amp design, the impossibility of employing complementary stages at the op-amp input is not a serious problem when the amplifier has an inverter configuration, since a differential pair can be employed (e.g. a PMOS) keeping the common-mode input voltage of the amplifier very close to one of the supply voltages (the lowest one for the PMOS case) of the circuit. By using a periodic charge injection in SC circuits [37], [38] or a DC level shift in continuous-time circuits [39], the difference between the common-mode voltages at the input and the output of the op-amp that allows a maximum output voltage range can be solved. However, in non-inverter circuits, a technique to remove the common-mode component of an input differential signal is proposed in [40], and the same effect is achieved in [41], [42] in a more efficient and simpler way.

At this cell level, new concepts have been developed in the past few years, aiming to have great impact reducing voltage and power in analog and mixed-mode circuits. Among them, Floating Gate and Quasi-Floating Gate techniques, deeply explained in Chapter 2, are going to have a special relevance in this thesis. QFG techniques are based on using MOS devices with one or multiple inputs capacitively coupled to the gate terminal (like the Floating Gate devices, also explained in Chapter 2) but with the DC operating point set by a large resistor. These techniques allow eliminating the offset caused during fabrication, as well as achieving less area and a great potential for class AB operation. Some examples of the use of these techniques in common circuits like op-amps, OTAs or multipliers are [43–47].

Considering the reduction of power consumption, class AB stages have become very popular and even necessary in low-power circuits. They allow obtaining large Slew-Rate values for large-signal operation with low bias currents, so keeping low static power consumption. An interesting way of obtaining class AB operation in the output stages is by means of the already mentioned QFG techniques. This proposal is covered in Chapter 2 as well, and is applied in several papers like [26], [48–50].

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In relation to this class AB operation, super-class AB amplifiers have been recently proposed [51–53]. This concept is applied to one-stage amplifiers where class AB operation has been achieved both in the input differential pair and in the active load. By means of this technique, the obtained slew-rate is similar to conventional class AB amplifiers, while the static power consumption is reduced by one order of magnitude obtaining a power efficiency close to 100%.

Another interesting topic, widely researched lately, is the use of MOS transistors operating in moderate inversion [54–56]. By operating in this region, good performance in low-power circuits is obtained in terms of linearity, bandwidth and noise. Significant advantages can be obtained by combining both moderate (or even weak) inversion operation and FG or QFG configurations in a transistor.

Considering sub-system level, some remarkable contributions exist in the field of the SC circuits, such as the switched-opamp method proposed in [57], [58], based on the replacement of the critical switches of the conventional switched-capacitor technique with opamps, which are turned on and off, resulting in a true very low voltage operation. Another example is the employment of techniques of clock-amplification using the circuit presented in [59]. Moreover, companding techniques are also interesting nowadays in order to compensate for the reduction of the dynamic range in some circuits [60], [61]. Companding consists in exploiting the non-linear behavior of basic devices, like transistors, compensating globally their non-linearities, allowing in such a way for the biasing to set close to the limits imposed by the technology. Besides, by using this technique, wide current swings can be achieved with small voltage variations, improving speed and reducing supply voltage requirements [62]. These techniques have been validated in several circuits such as strong or weak inversion MOS circuits or bipolar topologies [63–65].

Furthermore, both in cell design and in systems or subsystems design, general current-mode techniques must also be highlighted [66–69], and more interesting for low-power designs are the ones using transistors in weak inversion region [70–72].

Finally, some examples of contributions at system level include, trying to reduce supply voltages or power consumption, improvements done in the field of A/D converters. It is necessary to choose the appropriate architecture [73] and, in order to achieve the required dynamic range in a compact and power-efficient way, the choice of Sigma-Delta converters [74], [75] and their implementation

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with a very low supply voltage [33] is almost mandatory. Other proposals, also useful for low-voltage designs due to their efficiency in terms of power consumption, are [76], [77].

1.1.2 Gm-C Filters

As it has been already said in this Section, Gm-C filters have replaced progressively classic MOSFET-C and RC realizations in many applications due to their wider frequency response, despite the drawback of the poor linearity inherent to traditional OTAs. Precisely, as specified before, the implementation of Gm-C filters is the goal of this thesis. Obviously, in order to be competitive in the target application, linearity of Gm-C filters must increase by means of several techniques, like input attenuation, or source degeneration, or another one of the methods explained later in Chapter 3 [78].

First of all, Gm-C filters have needed to adapt themselves to the previously presented changes that technology and power supply have suffered over the years. For instance, while at the beginning of the 90s, filters were implemented with technologies like CMOS 0.9 μm [79] or high power supplies like 10V [80], actual filters employ more modern technologies, like CMOS 90 nm [81], and lower power supplies, like 1V [21].

Regarding linearity improvement, Gm-C filters have used different approaches over the years, achieving performances comparable to those of RC configurations. Many filter topologies increase their linearity thanks to the source degeneration technique, like [17], [23], [27], [79], [82–92]. Among them, [17], [27], [82], [87], [88], [90] employ passive resistors in their designs which perform the V-I conversion, while other proposals like [79], [84–86] make use of triode transistors in order to degenerate the source. Other circuits use mixed source degeneration structures formed by both, passive resistors and MOS transistors in triode region [23], [89], [92], achieving at the same time high linearity and tunability. It must be noted that the first reference to the use of common-mode sensing by two matched degeneration devices can be found in [85]. Another method to linearize a filter, also explained deeply in Chapter 3, is the adaptive biasing, employed in filters like [93], [94]. A combination of both linearization techniques can be seen in [83]. Lastly, it is also interesting to note that some topologies, like the ones proposed in [80], [87], [90], use passive feedback components as for the active RC configurations, so the resulting filters are considered as hybrids between Gm-C filters and active RC circuits providing a good tradeoff between linearity and bandwidth.

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Moreover, by analyzing the state-of-the-art of Gm-C filters, some topologies already employing Floating Gate and Quasi Floating Gate techniques in their designs can be discovered. On the one hand, some proposals like [17] present a FGMOS as input transistor, showing an improvement of linearity up to 10 dB in comparison with an equivalent circuit without FGMOS. In [46], [55], [95], [96] FGMOS transistors have also been used in the design of multiple-input transconductors as a way to finally implement very low-power filters. On the other hand, QFG techniques have also been used in some topologies such as [97], in order to linearize triode transistors in source degeneration structures and achieve an ideal cancellation of the non-linear terms of the equivalent resistor. Proposals like [98], [99] also use QFG transistors in their implementation. Article [100] shows how to apply FG and QFG techniques in different circuit implementations and the advantages they provide. Besides these interesting techniques, other strategies also mentioned in the previous Section, have been applied to transconductor blocks at transistor level in order to achieve low-voltage low-power operation in Gm-C topologies [36], [101–103].

Considering the topology and the design of Gm-C filters, several strategies can be followed, including the biquad cascade [86], [104], LC ladder simulation -substituting passive inductances by gyrators- [20] and multiple loop feedback [105]. The following books about filter designs propose different techniques [25], [106], [107].

Finally, regarding tuning, different methods have been employed over the years in Gm-C filters design. While some topologies choose discrete frequency tuning configurations like capacitor arrays [92], [108] or switchable transconductors [109], [110], other filters use continuous tuning schemes instead. Different continuous approaches can be discovered by looking throughout the literature such as tuning based on multipliers [80], transconductance tuning by external resistors in charge of setting the bias currents [44], [88], [91] or manual tuning by changing directly the bias current [111], [112]. Another proposal, of great relevance for this work, consists in implementing a resistive divider with triode transistors in order to tune the circuit. This idea, firstly proposed in [90], has also been used in [17], [82], [83]. Furthermore, in some cases automatic tuning circuitry is also included on the same chip in fully integrated Gm-C filter design, in order to overcome the effects of parameter drift due to the process, temperature and environment variations or aging. Among others, Master-Slave automatic tuning with VCO or methods based on charge balancing and Gm-C

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integrators have been employed ([20], [23], [79], [85], [87], [90], [104], [110], [113–115]).

1.2 Objectives

According to what has been said so far, the general purpose of this thesis is to develop circuits and techniques for Gm-C filter design, focusing the efforts on achieving for them low-voltage and low-power operation. In particular, the objectives of this work are the following:

At cell level:

❖ At this level, the first objective is to summarize the state-of-the-art of the main low-power low-voltage techniques employed so far in the literature. Mainly, this analysis is going to be focused on techniques based on Floating Gate (FG) and Quasi-Floating Gate (QFG) transistors.

❖ To apply these low-power low-voltage techniques in order to design basic cells -transconductors mainly- suitable for Gm-C filter design. Special attention must be paid, when these techniques are applied, to the performance of the circuits, particularly in terms of power consumption and linearity.

❖ To develop a systematic approach to implement high-performance CMOS tunable transconductors able to fulfill the challenging requirements of current analog design.

At system level:

❖ To perform a general overview of different wireless receiver configurations, paying special attention to homodyne receivers, which are going to include in their implementation the circuits proposed in this work.

❖ To summarize the advantages and drawbacks of using Gm-C filter topologies in modern communication systems, as well as provide solutions to

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overcome the issues they present. The evolution suffered by this type of filters in analog design must also be studied.

❖ To implement a tunable highly linear third-order Butterworth low-pass Gm-C filter suitable for both Bluetooth and Zigbee applications by employing some of the techniques at both basic cell and system level proposed throughout this work.

❖ To propose some Automatic Tuning Systems, appropriate to be used along with the implemented filter, in order to make it more practical and better adapted to current necessities.

❖ To implement other important blocks of the receiver by means of the previously obtained transconductor and the low-voltage low-power techniques, like the VGA. An offset-cancellation circuit is usually necessary when the VGA presents multiple stages.

By fulfilling these objectives, this thesis tries to contribute to low-voltage low-power continuous-time filtering at both cell and system level, which is one of the most important trends in analog design due to the huge proliferation of wireless devices, as well as to wireless reception in general by implementing other necessary low-power blocks. All the circuits developed in this work have been fabricated and tested using a 0.5μm n-well CMOS technology.

1.3 Structure of the Thesis

This thesis is organized in six chapters, being the first one the present introductory chapter. It has been focused on explaining the motivations of this work, along with an overview of low-voltage low-power techniques and a summary of the state-of-the-art of Gm-C filter design. Besides, the objectives of the thesis have been established. The following paragraphs provide a summary of the other five chapters of this work.

Chapter 2 covers the concept of Floating Gate (FG) and Quasi-Floating Gate (QFG) transistors. These two devices are analyzed in detail in this chapter, as well as several techniques based on them. Some applications, where these

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techniques are employed, are also presented. This chapter is particularly relevant for this thesis, as many of the proposed techniques are going to be applied throughout it in order to achieve low-voltage and low-power operation, but also to provide tuning capability or linearity improvement.

Chapter 3 is devoted to the design technique of high-performance CMOS transconductors, challenging nowadays due to the restrictions imposed by technology downscaling and low power requirements. To overcome these current issues, techniques presented in Chapter 2 are going to be employed in the design. Several circuit configurations are proposed throughout this chapter. By having their performances compared, the most suitable ones to implement a proper transconductor can be chosen. In fact, this chapter also provides a systematic approach to implement suitable transconductors for wireless receivers, resulting in a new family of cells featuring high linearity in a wide input range, class AB operation and continuous tuning.

In Chapter 4, focused on Gm-C filter design, a wide range tunable highly linear third order Butterworth low-pass Gm-C filter is implemented and fabricated, using the systematic approach proposed in the previous chapter to obtain its basic cell, a class AB programmable transconductor. QFG techniques are also employed in the design. Measurements results can be found in this chapter. Furthermore, an optimized version in terms of area of this Gm-C filter is implemented as well. Lastly, two Automatic Tuning Systems are proposed to operate along with the filter, making it more practical.

Chapter 5 is devoted to implement other important blocks of a wireless receiver, employing for it the basic transconductor cell previously proposed and verified. According to this goal, a Variable Gain Amplifier (VGA) is proposed, fabricated and measured. This circuit operates with constant bandwidth for all the gain settings. Moreover, from the experimentally validated one-stage VGA, a three-stage VGA is also proposed. The aim of this new circuit is to achieve a larger gain tuning range than the basic one. Nevertheless, an offset-cancellation circuit is now necessary and must be added. A proposal is included to this aim.

Finally, Chapter 6 provides a compilation of the most significant results and general conclusions of this work. Besides, future research lines related to this thesis are proposed and briefly analyzed.

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CHAPTER 2

Low-voltage and low-power design techniques

Nowadays, current trend in circuit design is towards devices featuring at the same time low-power consumption and very low-voltage supplies in order to satisfy the requests of wireless communication technologies and portable devices and to deal with the downscaling that CMOS technology is suffering in the last decades [1]. These supply voltages are getting even close to the thresholds voltages of MOS transistors, which scale down with a lower rate than them. Due to this continuous technology scaling, systems are having some issues related to power consumption, as well as suffering a rise in the on-chip integration density, hence raising the cost of packaging [2]. Particularly, in the case of CMOS analog circuits using conventional techniques, this drastic reduction of supply voltages means both degradation in terms of its dynamic range and its signal-to-noise ratio [3]. As a consequence, low-voltage low-power designers face a real technological challenge, as they must take into account the multiple and, usually, opposed demands of current devices and systems.

In order to solve the problems caused by this trend, novel alternative design techniques have been developed since the beginning of the 90s. Specifically, these new techniques are aimed to work with low voltage supplies and with rail-to-rail signals. Those techniques employed in analog design have been changing throughout the years, but their main goal has remained constant all along the time, achieving power-aware designs. We can find many publications

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emphasizing the importance of power consumption [4–9], as well as showing the measures taken to reduce it [10].

Two of these mentioned techniques, on which the circuits implemented in following chapters are going to be based, are the Floating-Gate (FG) [9], [11–13] and Quasi-Floating Gate (QFG) [3], [14–16] techniques, widely used in analog design. By employing them, there are nowadays new possibilities in analog design that allow achieving more accurate and improved devices. Some examples of these improvements are class AB operation or rail-to-rail input range [16].

The aim of this chapter is to analyze how these techniques can be applied to analog design, such as in the implementation of CMOS transconductors developed in following chapters. Several up-to-date applications employ these transconductors, like continuous-time filters, A/D and D/A converters or variable-gain amplifiers (VGAs) [17], [18]. The design of these devices is complicated, as it presents different issues to deal with, like limited signal swing or limited linearity. By means of the aforementioned techniques these drawbacks can be overcome.

In Section 2.1 the fundamentals of Floating-Gate techniques are going to be discussed, while Section 2.2 is going to be focused on Quasi-Floating Gate techniques. Finally, Section 2.3 deals with the application of both to achieve rail-to-rail input range or class AB operation, among other things.

2.1 Floating Gate MOS Transistor

A Floating-Gate MOS transistor, which is going to be named throughout this thesis as FGMOS transistor, is a device where the voltage of its gate terminal is not controlled directly, as opposed to conventional MOS transistors.

A FGMOS transistor of n inputs is characterized by having a polysilicon gate, spread out over the channel, floating in DC, but capacitively coupled to the different inputs using a second polysilicon layer which forms the poly-poly input capacitors, C_n. Usually poly1 is used for the floating gate, while poly2 is chosen for the second layer, because their overlap results in high quality capacitors. Figure 2.1 shows the layout and symbol of a two-input FGMOS transistor.

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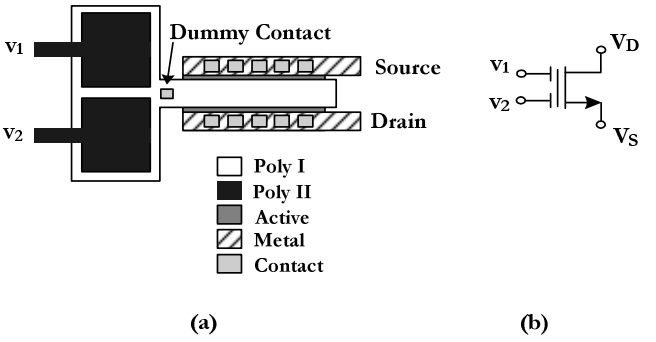

Figure 2.1. Two-input FGMOS transistor. (a) Layout (b) Symbol

The equivalent circuit of an n input FGMOS transistor is represented in Figure 2.2. The capacitive couplings between the n inputs and the floating gate terminal of the transistor, as well as the parasitic capacitances, are shown in this figure.

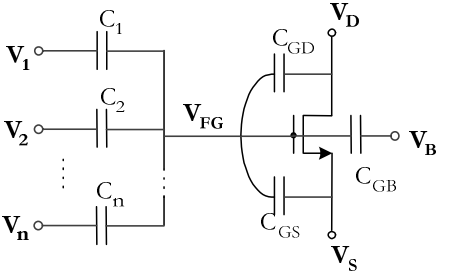

Figure 2.2. Equivalent circuit of an *n* input FGMOS transistor

Theoretically, the floating gate of a FGMOS transistor is not able to charge or discharge itself and, as a consequence, the initial charge stored in it will be preserved. Therefore, the floating gate voltage of the transistor has the following expression [19]:

$$V_{FG} = \frac{1}{C_T}\left(\sum_{i=1}^{N} C_i V_i + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B + Q_0\right) \qquad (2.1)$$

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where $C_T = \sum_{i=1}^{N} C_i + C_{GS} + C_{GD} + C_{GB}$ and Q_0 is the initial charge trapped in the floating gate. This charge could produce undesired DC offsets or large variations of threshold voltage.

This accumulated charge can be removed during fabrication, if appropriate layout techniques have been applied or, as it has been done traditionally, by using UV radiation, like in EPROM memories, once the circuit is already fabricated. A different technique to solve the trapped charge problem without extra mask or processing costs is proposed in [11]. It is based on adding a polysilicon to metal contact on the floating gate, stacking all the contacts available in the process for the different metal layers. As the floating gate remains isolated from any other part of the circuit, given that the contact stack does not create any new connection, its functionality remains constant. During deposition of each metal layer and before selective etching, all the nodes sharing this layer are connected to the floating gates, interconnected via the metal layer, offering a low-impedance path that discharges them. After having etched the final metal layer, the floating condition of the gates, lost during this process, is restored.

As it can be deduced from (2.1), the floating gate voltage of the FGMOS transistor is a weighted addition of the n input voltages, where each input voltage coefficient is the ratio between its coupling capacitance C_k and the total capacitance C_T connected to the floating gate, and some additional terms due to parasitic capacitances.

$$V_{FG} = a_1 \cdot V_1 + \cdots + a_n \cdot V_n + \frac{C_{GS}}{C_T} \cdot V_S + \frac{C_{GD}}{C_T} \cdot V_D + \frac{C_{GB}}{C_T} \cdot V_B \qquad (2.2)$$

$$a_k = \frac{C_k}{C_T} \qquad (2.3)$$

Therefore, input voltages suffer attenuation, due to the capacitive voltage dividers and, as a result, rail-to-rail input signals can be employed. In fact, the capacitive voltage divider of these devices allows both scaling and level shifting of the input voltages. This is a very important achievement for low supply voltage applications.

2.2 Quasi-Floating Gate MOS Transistor

One important requirement, in order to bias correctly an FGMOS transistor so as to use it in low-voltage applications, is keeping the DC voltage of

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the floating gate close to one of the rails. It should be near V_{DD} if the transistor is NMOS or near V_{SS} if it is PMOS. In view of the above a light transformation of the FGMOS circuit shown in Figure 2.1 and 2.2 must be done. Figure 2.3 shows the resulting device.

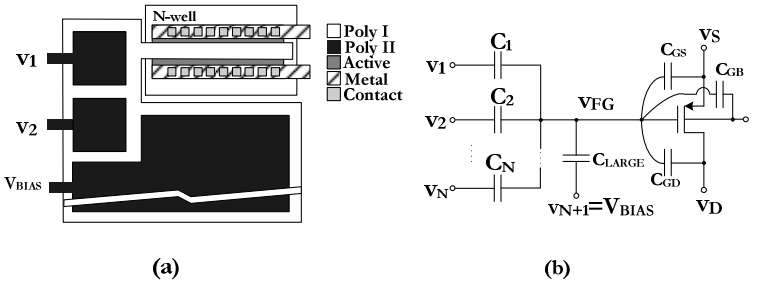

Figure 2.3. Multiple-input FGMOS transistor. (a) Layout (b) Equivalent circuit

The addition of input v_{N+1} is the main difference between both equivalent circuits. This new input is going to be a DC voltage, called V_{BIAS}, and its value will be either V_{DD} or V_{SS} depending on the type of transistor, as it has been already explained. The floating gate voltage of the transistor has now the following expression:

$$v_{FG} = \frac{C_{LARGE}}{C_T} V_{BIAS} + \frac{1}{C_T}\left(\sum_{i=1}^{N} C_i v_i + C_{GS} v_S + C_{GD} v_D + C_{GB} v_B + Q_0\right) \quad (2.4)$$

As it can be seen, a large capacitance ratio is needed in order to achieve a floating gate voltage close to one the rails, and that means that a large coupling capacitor C_{LARGE} is required, much larger than the rest. As a result, besides the inherent trapped charge problem of FGMOS transistors, this device presents some new drawbacks. Not only the required silicon area has increased considerably, as Figure 2.3 shows, but also the Gain-Bandwidth (GB) product can suffer a reduction when FGMOS transistors form the input differential pair of an amplifier.

All these issues can be solved by using a large resistor to connect the floating gate to the DC bias voltage, instead of the C_{LARGE} previously employed. By means of this substitution, a Quasi-Floating Gate MOS transistor has been

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obtained, which is going to be named from now on as QFGMOS transistor. The layout and equivalent circuit of a 2-input QFGMOS transistor are shown in Figure 2.4 [3].

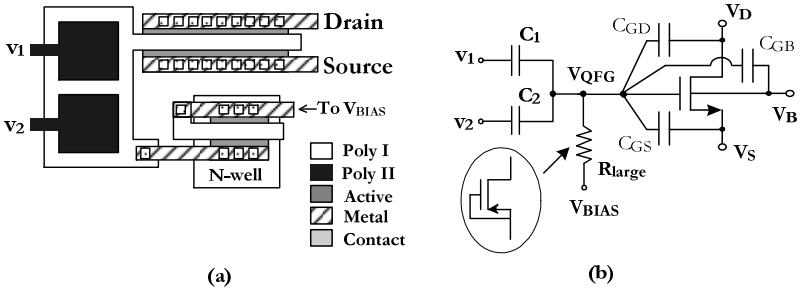

Figure 2.4. Two-input QFGMOS transistor. (a) Layout (b) Equivalent circuit

Like in the case of FGMOS transistors, inputs are capacitively coupled to the gate terminal but, this time, the gate is also weakly connected to a DC voltage through a large resistor. Typically, this resistor is implemented by the leakage resistance, R_{LARGE}, of a reverse-biased p-n junction of a diode-connected MOS transistor operating in cutoff region, as it can be seen in the inset of the previous figure. The size of this MOS transistor can be minimal, saving area as compared to Figure 2.3. As a consequence of these connections of the gate, it becomes a Quasi-Floating gate, turning the transistor into a QFGMOS one. The DC voltage of this QFGMOS device will be set to V_{BIAS} independently of the different DC voltages of the input signals.

Considering AC operation, the quasi-floating gate voltage of an n input QFGMOS transistor is:

$$V_{QFG} = \frac{sR_{large}}{1+sR_{large}C_T}\left(\sum_{i=1}^{N} C_i V_i + C_{GS}V_S + C_{GD}V_D + C_{GB}V_{bias}\right) \qquad (2.5)$$

where C_T now includes the parasitic capacitance of the large valued resistance seen from the gate.

According to expression (2.5), inputs experience a high-pass filtering with a cutoff frequency $1/(2\pi R_{LARGE}C_T)$, which can have very low values (below 1 Hz). So, even for very low frequencies, expression (2.5) becomes a weighted addition of the AC input signals determined by ratios between capacitances, plus some parasitic terms. It must be highlighted that the exact value of R_{LARGE} as well as its dependence on voltage or temperature are not

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relevant, as long as the value of the resistance remains large enough so as to achieve a cutoff frequency lower than the lowest signal frequency required. For the same reason, the exact value of C_T is not important either.

2.3 Applications of FGMOS and QFGMOS techniques

In order to implement CMOS transconductors and Gm-C filters in an efficient way, this section is going to illustrate some applications of FGMOS and QFGMOS devices. The techniques achieved thanks to them are very useful for low-voltage and low-power operation.

2.3.1 Rail-to-Rail Input Range

Nowadays, as the current trend in analog design is towards very low-voltage circuits, input range has become one of the most limiting features, and its enlargement has been studied extensively [9], [13], [20–22]. Conventionally, by diminishing the supply voltages, the voltage headroom available at the inputs decreased as well so as to keep the input transistors properly biased. However, FGMOS transistors are going to help in extending the input range until rail-to-rail operation, allowing obtaining maximum dynamic range at limited supply voltages. The method is shown in Figure 2.5.

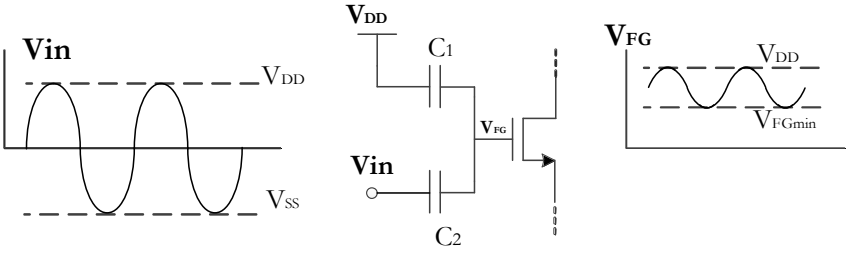

Figure 2.5. Rail-to-rail operation with FGMOS techniques

According to the figure, the input voltage is connected to the floating gate through a capacitor, C_2, while the supply voltage is connected to it through another, C_1. As a consequence, one of the inputs is in charge of the biasing of the circuit and the other of the signal processing. As a result, the capacitive divider provides both signal scaling and DC level shifting, features that allow obtaining a rail-to-rail input range despite the limited voltage range available at the gate.

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Figure 2.5 shows this transformation of the original signal into a downscaled and shifted version of itself for a two-input n-type FGMOS transistor.

The floating gate voltage of this specific case can be obtained from (2.1), assuming zero initial charge and neglecting parasitic capacitances:

$$V_{FG} = \frac{C_1}{C_1 + C_2} V_{DD} + \frac{C_2}{C_1 + C_2} V_{in} \qquad (2.6)$$

The input signal is attenuated by a factor $a = C_2/(C_1 + C_2)$ and up-shifted by a DC voltage $V_{DC} = V_{DD}C_1/(C_1 + C_2)$. Note that when V_{in} is equal to V_{DD}, V_{FG} is also equal to V_{DD}, but when V_{in} is equal to V_{SS}, V_{FG} depends on the ratio of the capacitors C_1 and C_2. So, it is very important to choose the proper values for them in order to achieve rail-to-rail operation, while the transistor remains properly biased by keeping a floating gate voltage high enough. For a p-type FGMOS transistor, where a DC down-shifting is required, the process is similar except for the DC voltage supply connected to C_1 that must be V_{SS}.

The input attenuation reduces the signal swing and, as a result, linearity improves. However, input-referred noise voltage is also increased by a factor $1/a$. This technique has been used in many different circuits such as op-amps or transconductors, [13], [23], [24].

2.3.2 Linearization of Active Resistances

Usually, analog systems based on transconductors, like Gm-C filters or VGA, require continuous tuning in order to adjust its transconductance value. This is interesting not only to reach the exact desired values of some parameters for a specific application, like a particular cutoff frequency or bandwidth, but also because the most likely thing is that, after fabrication, the real values of the components do not match with those fixed in simulation, so to obtain the desired results, a final adjustment will be needed. Besides, circuits suffer changes due to process and temperature variations that tuning can compensate as well.

Achieving tunable circuits is not trivial and the design must be done carefully because an inefficient tuning can degrade the performance of the whole circuit. There are many different tuning strategies, depending on what suits the designer better. Among the possibilities [25], Figure 2.6 shows one conventional approach.

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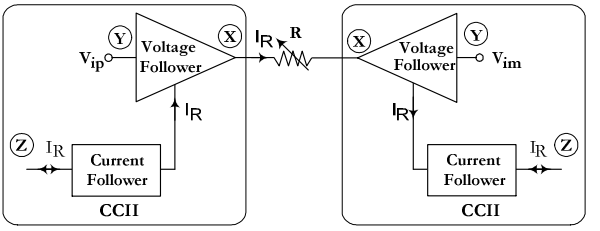

Figure 2.6. Transconductor tuning: Adjusting the resistor used for V-I conversion

This figure presents the implementation of the transconductor employed in this strategy. Voltage-to-current conversion is based on two second-generation current conveyors (CCIIs) and passive resistors R. A CCII [26] is a three-terminal device where voltage at the high-impedance terminal Y is copied to the low-impedance terminal X, and current in terminal X is copied to the high-impedance terminal Z. Thus, in the proposed transconductor the differential input voltage is replicated at the terminals of resistor R by the input voltage followers, achieving a highly linear V-I conversion. The resulting resistor current I_R=Vid/R is conveyed to the high-impedance Z output by two current followers. Transconductors implemented with passive resistors in such a way are widely used since they can provide high linearity [25] and, at the same time, small sensitivity to second-order effects.

Figure 2.6 shows the simplest tuning strategy. In this case, the transconductor tuning is based on changing the value of the resistor in charge of the V-I conversion. By changing this resistance, the transconductance of the circuit is going to be modified as well. As the value of a passive resistor cannot be tuned, the use of this component must be avoided, losing therefore the high linearity reached thanks to it. Typically, variable resistors are implemented with MOS transistors operating in triode region, despite the consequent linearity degradation. The way to tune a circuit which makes use of these transistors is by modifying the voltage at their gate terminal, considered as the control voltage.

In order to linearize the resulting active resistance, besides the MOS transistor two capacitors and a large resistor are added to the circuit. The capacitors are in charge of connecting in AC the drain and source terminals with

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the gate terminal and the high-valued resistor, that connects the control voltage with the gate terminal, establishes V_{tun} as its DC voltage. As a consequence, by using QFGMOS techniques, linearity of the MOS transistor operating in triode region, and therefore of the V-I conversion, is improved. Figure 2.7 highlights this [27].

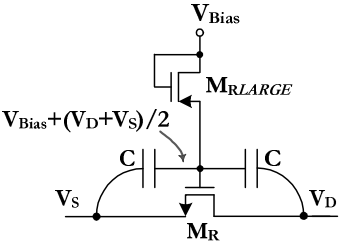

Figure 2.7. Triode transistor with enhanced linearity using QFG technique

Figure 2.7 shows a 2-input QFGMOS transistor in triode region as active resistor, where its DC gate voltage is set to V_{Bias} and can be adjusted to provide tuning. Moreover, due to the matched capacitors, the AC gate voltage is the common-mode voltage of the AC drain and source voltages, which leads to a linearity improvement. As it has been studied in [28], body-effect and mobility degradation both depend mainly on the common mode of the drain and source voltages, so linearity can be greatly improved by applying this common mode signal superimposed to the quiescent voltage to the gate.

From the expression of the current that goes through a MOS transistor in triode region, it can be understood how this circuit works so as to achieve a linearized response.

$$I_D = \beta \left[(V_{GS} - V_{TH}) \cdot V_{DS} - \frac{{V_{DS}}^2}{2} \right] \qquad (2.7)$$

The term $V_{DS}^2/2$ must be eliminated in order to achieve a linear expression and a linear equivalent resistance. As, according to Figure 2.7, the whole voltage at the gate terminal is:

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$$V_G = V_{tun} + \frac{V_D + V_S}{2} \qquad (2.8)$$

by replacing this expression in (2.7), the non-linear term is cancelled and the V-I relation is finally linear. In practice expression (2.7) is only an approximation and the linearity improvement achieved is limited.

2.3.3 Class AB Operation

In order to improve the performance of a circuit, so that it can fulfill the specifications of different applications, another technique employed in this work is the design of class AB operating circuits, instead of the commonly used class A ones. Class AB operation can be obtained by using previously explained QFGMOS transistors [29].

Figure 2.8 shows the basic class AB output stage with a floating battery, and the implementation of that battery by means of a QFGMOS transistor. Finally, an implementation of R_{LARGE} is illustrated.

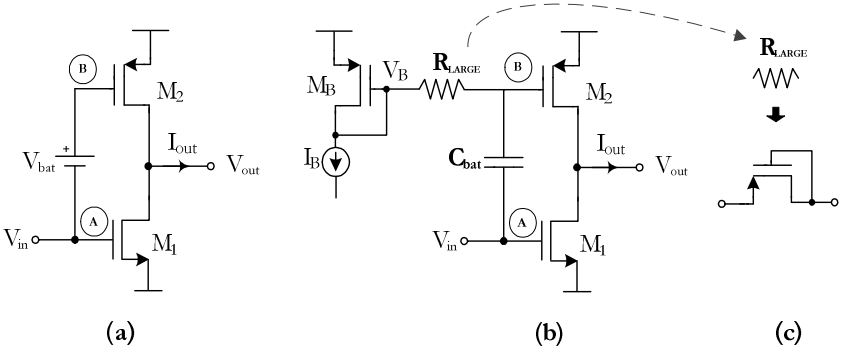

Figure 2.8. Classic class AB output stage (a) Floating battery implementation (b) QFGMOS implementation (c) Implementation of R_{LARGE}

By using a floating battery in the class AB amplification stage of Figure 2.8 (a), node B is able to follow the voltage variations of node A with a DC voltage difference of V_{bat} Volts. Lacking of signal, current is determined by node A voltage plus V_{bat} DC voltage. However, in dynamic conditions, signal changes in node A are transferred to node B, allowing the output current not to be limited by the quiescent current. The DC level shift has been implemented in several ways, for instance using diode-connected transistors or resistors biased by DC

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currents. However, these solutions require extra quiescent power consumption and may increase supply voltage requirements. Besides the quiescent current is often not accurately set and dependent on process and temperature variations, and the parasitics added by this extra circuitry may limit bandwidth.

Figure 2.8 (b), where a QFGMOS transistor has been used to implement the floating battery [30], shows that the output current in the absence of signal is I_B, due to the capacitor behavior as an open circuit in DC which leads to a setting of the current by means of the PMOS transistors current mirror, so regardless of thermal and process variations. As it has been previously said, under dynamic conditions, node A voltage is transferred to node B, but after being attenuated by a factor $C_{bat}/(C_{bat}+C_B)$ and high-pass filtered with cutoff frequency $1/(2\pi R_{LARGE}(C_{bat} + C_B))$, where C_B is the capacitance of node B. In view of the large resistance value, the cutoff frequency is going to be very small, typically below 1Hz, avoiding only the input signal DC voltage component to be transferred from node A to node B. According to Figure 2.8 (c), as it has been mentioned before, R_{LARGE} can be implemented by the reverse-biased p-n junction of a diode-connected MOS transistor operating in cutoff region, so the silicon area increase, inevitable in class AB circuits, is quite modest.

One of the main advantages of the class AB operation of the circuit is the significant improvement of the Slew-Rate while *large-signal* operation. The Slew-Rate expression, considering C_L as the output capacitive charge, is shown here:

$$SR_+ = \frac{I_{out}^{max}}{C_L} \qquad (2.9)$$

During *large-signal* operation, a large amount of current is needed at the output capacitor in order to achieve a large output voltage. Obviously, in such a case the Slew-Rate parameter is going to be highly affected by the current achieving the capacitor. The more current charges the capacitor, the quicker the charge takes place, and the larger the Slew-Rate is.

Using class AB operating circuits, the output current is not limited by the aforementioned bias current, I_B. As a consequence, this bias current does not need to be increased in order to achieve large current values at the output. Therefore, a large Slew-Rate can be obtained for *large-signal* operation with low I_B values, so keeping low power consumption as well.

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2.4 Summary

This chapter summarizes some of the techniques employed nowadays by analog designers in order to obtain circuits featuring both low voltage and low power consumption. Focus has been on FGMOS and QFGMOS techniques, which will be employed in this thesis. Their way of functioning has been explained along this chapter, as well as some applications obtained thanks to them.

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CHAPTER 3

Tunable class AB transconductor design for wireless receivers

Due to the increasing and varied demands of modern wireless communication systems, the design of high-performance continuous-time analog circuits has become a technological challenge. Nowadays, the current trend is using more elaborated modulation schemes with higher data rates, even if they require larger bandwidth and high linearity for their receiver front-end circuits and their analog filters. As an example, several current communication systems like ADSL, VDSL, 802.11a/g wireless LANs, WiMax, or DVB, use multicarrier modulation schemes. These schemes are based on employing multiple carriers over a wide bandwidth to provide robustness against the impairments of poor quality wireless communication channels, and require high linearity in a wide bandwidth to avoid intermodulation distortion among the carriers [1], [2].

Although active-RC continuous-time filters are widely employed for these demanding applications due to their high linearity and their high Signal-to-Noise ratio, also transconductance-C (Gm-C) topologies have been proposed [3–6]. Unlike active-RC topologies where the bandwidth is limited to a few MHz due to their closed-loop operation, Gm-C filters reach higher frequencies. Due to their open-loop operation, they usually achieve lower power consumption for a given bandwidth, but they also feature less linearity. In order to solve this limitation, the basic trend is designing the transconductors by coming back to the

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classic approach to achieve highly linear circuits, by the use of negative feedback and passive resistors, providing a highly linear voltage-to-current (V-I) conversion. This way, linearity levels comparable to those of active-RC filters have been reported [1], [7–9].

This chapter aims to analyze how Gm-C filters can obtain similar linearity values as those achieved by active-RC topologies and, according to the results, how to implement appropriate transconductors for that specific filter configuration aimed to minimize power consumption. The distinctive features of the design will depend on the necessities of the particular communication system.

In Section 3.1 classical linearization techniques for transconductors are presented, followed by a comparison between Gm-C and active-RC topologies in Section 3.2. Section 3.3 is focused in possible topologies of transconductors, based on current conveyors. The purpose of Sections 3.4 and 3.5 is designing voltage followers in class A and class AB, respectively, and class A and class AB current followers are implemented in Sections 3.6 and 3.7. By employing these voltage and current followers, class AB current conveyors are obtained in Section 3.8. Different highly linear tuning schemes for transconductors are discussed in Section 3.9. Finally, Section 3.10 deals with the design of complete class AB transconductors, followed by the conclusions of the chapter in Section 3.11.

3.1 Classical linearization techniques for transconductors

Practical transconductors are nonlinear devices because they usually contain bipolar or MOS transistors in their implementation. As a result, the output current does not depend linearly on the differential input voltage as it is the case for an ideal transconductor, but instead many additional undesirable terms related to the input voltages appear in the expression. In general, the output current is given by

$$i_O(v_+, v_-) = (v_+ - v_-)g_m + \sum_{i=1}^{\infty} a_i v_+^i + \sum_{i=1}^{\infty} b_i v_-^i + \sum_{i=1}^{\infty}\sum_{j=1}^{\infty} c_{ij}\, v_+^i v_-^i \quad (3.1)$$

where the desired term is the first one, as it relates linearly the output current with the differential input voltage through the transconductance.

This section is devoted to describe different conventional techniques employed to linearize transconductors [10]. The main approaches are the input

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signal attenuation, the cancellation of non-linear terms, the source degeneration and the adaptive bias.

3.1.1 Input Signal Attenuation

The first strategy to linearize a transconductor, from expression (3.1), is by reducing the input signal. When the input signal is attenuated by a factor k, the linearity of the circuit improves while the voltage input range is kept large. This method allows achieving a linearized approximation of the output current.

$$i_O(v_+, v_-) \cong k(v_+ - v_-)g_m \qquad (3.2)$$

Several techniques can be used to implement the attenuation factor, k. The general idea is illustrated in Figure 3.1 (a), while (b) and (c) show two different approaches to obtain k.

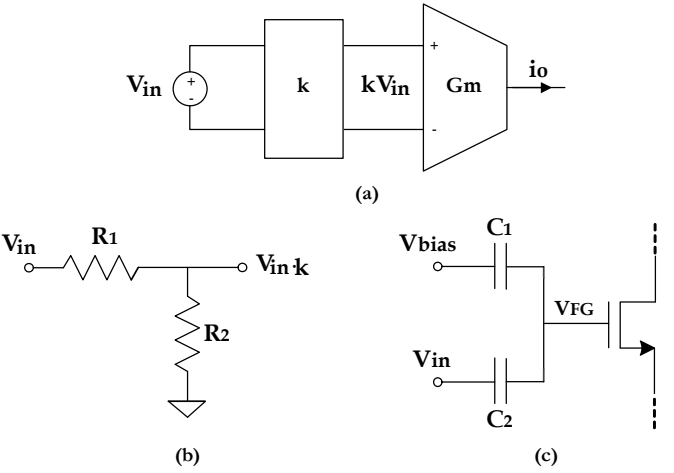

Figure 3.1. (a) Input Signal Attenuation (b) Using resistive divider (c) Using FGMOS techniques

The proposal of Figure 3.1 (b) is the attenuation of the input signal by a resistive divider. In this case k is equal to $R_2/(R_1+R_2)$. This technique is often used in commercial discrete OTAS. The second approach, proposed in Figure 3.1 (c), lies in attenuating the input signal by means of FGMOS techniques, that is to say, by a capacitive divider. As it has been said in the previous chapter, the floating gate voltage is

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$$V_{FG} = \frac{C_1}{C_1 + C_2} V_{bias} + \frac{C_2}{C_1 + C_2} V_{in} \qquad (3.3)$$

where the attenuation factor k is equal to $C_2/(C_1+C_2)$ [11], [12].

Nowadays, proposal (c) is mostly chosen over (b). By using FGMOS transistors the input is not resistively loaded, and the biasing is easier if one of the other capacitors connected to the floating gate is employed. Besides, the resistors add thermal noise. However, there are also some aforementioned disadvantages of using FGMOS transistors. The Signal-to-Noise ratio (SNR) is reduced considering that the noise generated by the transconductor is the same even if the input signal is attenuated and, as a consequence, the input referred noise is amplified by a factor 1/k.

As in all these linearized schemes the transconductor faces an attenuated input signal, the transconductance gain must be increased by the same factor in order to compensate it, increasing as well the silicon area and the power consumption.

3.1.2 Non-linear Terms Cancellation

An optimal algebraic sum of non-linear terms that results ideally in an only linear term is another option to linearize a transconductor [13–15]. The concept of this linearization is illustrated in Figure 3.2.

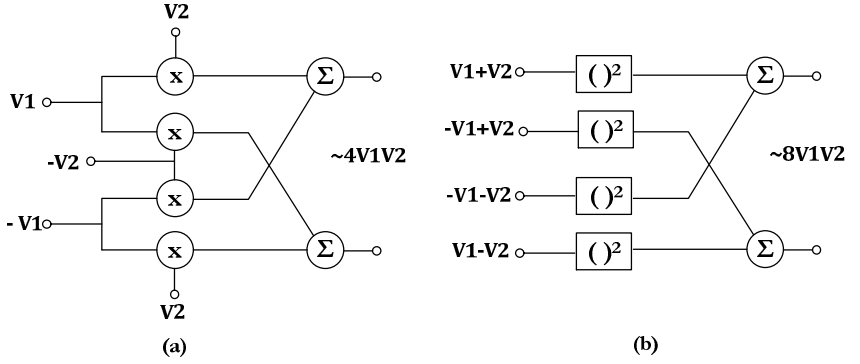

Figure 3.2. Transconductance linearization by non-linear terms cancellation
(a) Using single multipliers (b) Using single-quadrant devices

This can be achieved in practice by means of the interconnection of several transconductances, which ideally will cancel the non-linear terms yielding

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only a linear term that relates the input voltage and the output current. This same procedure is followed to cancel the even-order harmonics in differential circuits.

This technique is frequently used in the implementation of multipliers [16]. In these cases several terms of the transfer function are cancelled while a term representing the multiplication of the inputs remains. Figure 3.3 features an example of transconductors interconnected, acting as multipliers and using this linearization technique.

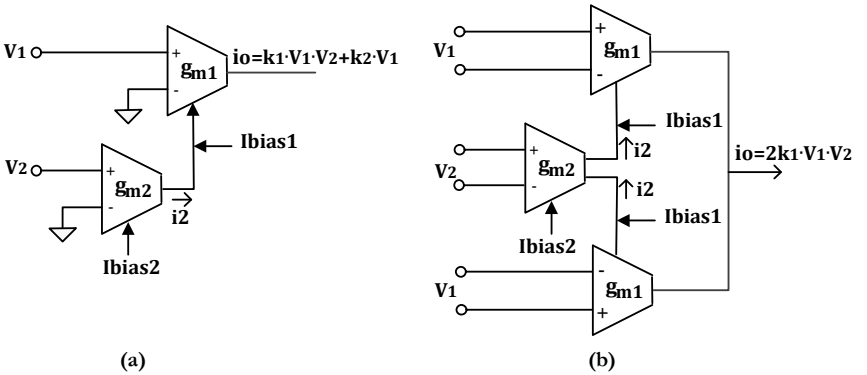

Figure 3.3. Multiplication operation (a) Without terms cancellation (b) With non-linear terms cancellation

In Figure 3.3 (a), the output current of transconductor g_{m1} is the addition of two terms, a linear one proportional to its input voltage, V_1, and a non-linear one that contains the multiplication of the two input signals. However, Figure 3.3 (b) shows how, by subtracting the undesirable linear term, the output current is proportional to the input signals multiplication, just as it is required.

This technique aimed to obtain multipliers [13] of the type of kxy, being x and y the input signals, is applicable also to linearize transconductors, where k is a multiplication constant and one of the inputs becomes a DC constant. An example is shown in Figure 3.4, where there is a practical implementation based on the circuit represented in Figure 3.2 (a). In this circuit with a fully differential configuration, bottom transistors operate in ohmic region while top ones operate in saturation in order to achieve the right transconductance. A DC bias voltage is needed at the input signals for proper operation.

The output current obtained from this circuit is

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$$I_O = I_{O1} - I_{O2} = (I_1 + I_3) - (I_2 + I_4) = 4kV_1V_2 \qquad (3.4)$$

as expected from Figure 3.2, after all the undesirable terms have been cancelled.

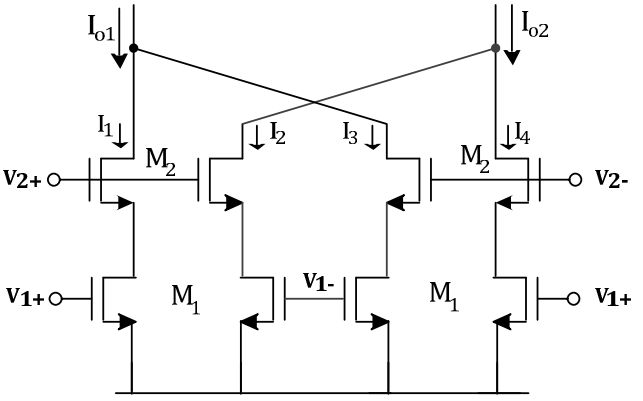

Figure 3.4. Transconductance based on Figure 3.2 (a)

Although it seems an interesting linearization method, this technique presents some important drawbacks. It strongly depends on the mismatch between transistors and on second order effects, like body effect, channel length modulation or other short-channel effects. Moreover, it is quite inefficient regarding power, as cancelled terms power is wasted.

3.1.3 Source Degeneration

One of the most commonly used linearization techniques is the source degeneration, achieved by introducing source degeneration resistors at the MOS transistors in order to have negative feedback with which an improvement of linearity takes place [10], [17–19].

Among the OTA topologies, the simplest one is a differential pair. Presuming matched transistors, its output current is equal to $G_m \cdot V_{in}$, but only in small-signal operation. When the input signal reaches a certain value, the small-signal operation loses its validity, linearity decreases and the output current saturates at the bias current value. According to this, the basic OTA presents high gain but small input range, an essential requirement for some applications like continuous-time filtering, employed in this thesis.

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As in most cases a larger interval of input voltages is required, the linear operation range should be expanded, so linearization is needed. The most common method is by introducing a resistive element between both source terminals of the differential pair transistors. In this way, output current is proportional to that one that goes through the resistor. Figure 3.5 shows both the basic OTA and two linearized versions.

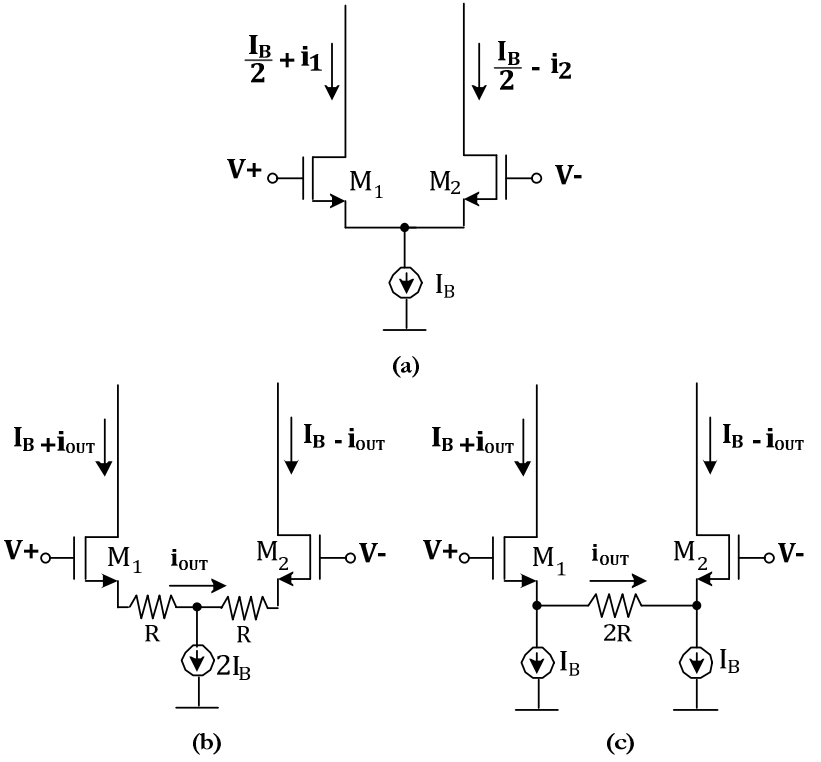

Figure 3.5. (a) Basic OTA (b),(c) Linearized OTA via source degeneration

In Figure 3.5 (b), where there are two resistors and an only current source between them, the noise generated by the source is going to appear at the differential outputs as common mode, so it can be cancelled. However, its useful input signal range decreases, as the bias current going through the resistors causes a voltage drop. Nevertheless, in Figure 3.5 (c) just the signal current goes through the degeneration resistor, allowing thus increasing the bias current without causing a reduction of the input range. Regarding noise, it is going to appear as a

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differential current, as it cannot be cancelled so easily as in (b). Moreover, in (c) mismatch problems are not as important as in (b). In both implementations, (b) and (c), the negative feedback achieved by the introduction of the resistors causes an attenuation of Vgs at the input transistors, which leads to a transconductance reduction and makes them operate in a tighter range near their operation point. Consequently, the linearity of the transconductance is improved. There are several techniques that can be used to implement the degeneration resistors, normally involving MOS transistors operating either in ohmic or in saturation region, like the ones presented in [15], [20], [21]. Assuming G_m the transconductance of M_1 and M_2, and $G_m>>1/R$, the following approximation can be obtained

$$G_{meff} = \frac{G_m}{1 + G_m \cdot R} \approx \frac{1}{R} \qquad (3.5)$$

To summarize, if the degeneration resistor is increased, feedback will end up also so much increased that the transistor is going to operate as a voltage follower and, as a consequence, transconductance will depend exclusively on the resistor value, a very useful and linear result. The disadvantage is that larger resistor means larger thermal noise, and that a larger G_m implies more power and/or area. Obviously, as the voltage to current conversion will depend on the transconductance, and at the same time, the transconductance depends on the resistor, the MOS transistor used to implement it should behave linearly.

According to this, it should be pointed out that the common mode sensitivity of the degeneration MOS resistors can be overcome by using the QFG techniques already explained in the previous chapter [18]. As a result, there is a significant linearity improvement and an enhanced CMRR, without needing an increase of supply voltages or additional quiescent power dissipation. Besides, it offers the possibility of tuning the MOS resistor value through small gate voltage variations. However, it requires additional hardware.

3.1.4 Adaptive Bias

Adaptive bias is another existing method to linearize a transconductor [22], [23]. This strategy is based on controlling the biasing of the input signal, in order to generate a specified bias current that contains non-linear terms capable of cancelling undesirable non-linear terms of the input signal. As a consequence, linearity improves. Nevertheless, as happened in the non-linear terms cancellation technique, linearity strongly depends on matching the different components.

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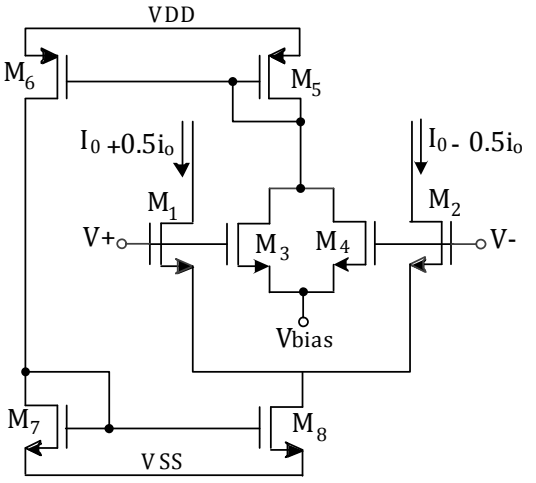

Figure 3.6. Adaptively biased MOS transconductor

Figure 3.6 shows an example of this technique. Being M_1 and M_2 the main transistors of the differential pair, the required biasing current can be easily obtained using another two MOS transistors, M_3 and M_4, with identical transconductance coefficients as them and two unit-gain current mirrors, M_5 and M_6 and M_7 and M_8. As it is highlighted here, matching is essential.

3.2 Gm-C versus Active-RC Topologies

As it has been already mentioned, active-RC filters achieve better linearity results than Gm-C topologies, although they have less bandwidth due to their closed-loop operation, as well as a higher consumption [24]. The reason is that active-RC topologies follow the classic design method to obtain stable, linear active circuits, which uses feedback and passive elements, and as a result, linearity only depends on the voltage coefficient of the passive components, supposing high enough gains of active devices, therefore it is very high. Figure 3.7 (a) shows a single-ended RC-integrator. A highly linear voltage-to-current (V-I) conversion takes place thanks to the virtual ground of the amplifier, and the current that goes through the resistor, V_{in}/R, is directly conveyed to the integrating capacitor.

In order to solve the linearity issue of Gm-C filters, it is necessary that the transconductors that define them present better linearity values. According to the previous section, there are several proposals to linearize a transconductor, like input attenuation employing FGMOS transistors, source degeneration, non-linear

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terms cancellation or a combination of some of them [10]. Techniques based on non-linear terms cancellation require accurately matched MOS transistors. The main problem of these techniques is their sensitivity to second-order effects that affect their transistors, like bulk effect, channel-length modulation or other short-channel effects, which cause a degradation of linearity.

In order to solve this limitation, the basic trend is designing the transconductors by coming back to the classic approach to achieve highly linear circuits, by the use of negative feedback and passive resistors, providing a highly linear voltage-to-current (V-I) conversion [7], [8], [25], [26]. This way, linearity levels comparable to those of active-RC filters have been reported [1]. By using this design technique, the resulting implementation of the transconductors of G_m-C filters will include at the same time high-gain active circuits, feedback loops and passive components, turning the filter into a hybrid between a G_m-C filter and an active-RC topology. This hybrid filter offers a good tradeoff between linearity, bandwidth and power consumption. In Figure 3.7 (b) a G_m-C integrator designed following this technique is shown. In fact, as a first-order low-pass filter is just an integrator with losses, a resistor, or a second transconductor acting as one, needs to be added to implement those losses in order to obtain a G_m-C filter.

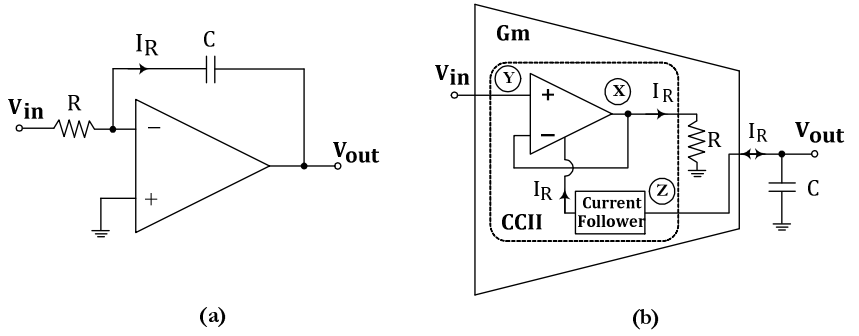

Figure 3.7. (a) Active-RC integrator (b) Highly linear Gm-C integrator

According to the figure, it is not exactly an open-loop topology and it works similarly to the active-RC circuits: firstly an accurate V-I conversion takes place by means of passive resistors and feedback amplifiers, and then the current is transferred to the capacitor in charge of integrating it.

Analyzing step by step Figure 3.7 (b), firstly a feedback amplifier has been employed to implement a voltage follower, in charge of transferring

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accurately the voltage from the input terminal (Y) to the resistor terminal (X). Consequently, the current at the resistor is equal to:

$$I_R = \frac{V_{in}}{R} \tag{3.6}$$

Typically, the conversion resulting current is already available at a high-impedance output node. However, with the intention of increasing the output voltage swing and achieving additional output impedance, a current follower is added after the conversion to carry the resulting current to the integrating capacitor. Therefore, this current follower, after having sensed the current at the low-impedance input (X), conveys it to the high impedance one (Z).

The voltage follower and the current follower altogether form a Second-Generation Current Conveyor (CCII) [27–29]. Current Conveyors are basic building blocks in many current-mode circuits, and are considered nowadays as extremely versatile analog building blocks. In order to use them for VLSI applications, so widely used nowadays, CCIIs should be designed in CMOS technologies and should operate with low supply voltage and power consumption. They are three-port structures, X, Y, and Z, and they work accordingly to the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & M & 0 \\ 1 & 0 & 0 \\ 0 & N & 0 \end{bmatrix} \cdot \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{3.7}$$

where I_X, I_Y, I_Z, V_X, V_Y, and V_Z are the currents and voltages of the respective terminals. There are three types of current conveyors depending on the value of constant M, namely CCI (M=1), CCII (M=0) and CCIII (M=-1). For each type, there are two subtypes, positive (CCI+, CCII+ and CCIII+) when N=1 and negative (CCI-, CCII- and CCIII-) when N= -1. This work will be focused on CCII structures, being the most widely employed.

As a consequence of the previous explanation, the transconductor of the G_m-C integrator illustrated in Figure 3.7 (b) is just a CCII with a resistor load in charge of converting the voltage into current. Besides, G_m-C filters obtained following this method can be considered, in a non-rigorous sense, as active-RC filters, where the CCII with internal feedback is the active element instead of an amplifier.

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The approach of Figure 3.7 (b) has some advantages with respect to other possibilities like the use of amplifiers, represented in Figure 3.7 (a). Firstly, by employing unity-gain local feedback, instead of feedback surrounding the complete device, the bandwidth increases. Moreover, the negative impact that continuous tuning has on linearity is lower in these circuits. This is due to the fact that, in active-RC filters, in order to obtain a continuous tuning, the passive resistor in charge of the V-I conversion must be replaced by an active implementation, usually a MOS transistor operating in triode region. As a result, linearity decreases, and dynamic range in case of low supply voltages is limited. On the other hand, as in G_m-C filters the copy of the resistor current obtained after the follower is sensed at a high impedance node, it can be scaled without affecting the V-I conversion that takes place at the passive resistor, thus allowing a highly linear continuous tuning.

3.3 Transconductor Design based on Passive Resistors

Taking Figure 3.7 (b) as a starting point, several implementations of transconductors can be designed. All of them are going to include CCII circuits in a differential configuration and, consequently, a light increase of power consumption will take place, although also a greater rejection of the common mode as well as less even-order distortion. Moreover, passive resistors will be in charge of the V-I conversion in all cases. The linearity of each implementation will depend on the efficiency achieved copying the voltages and the currents between the terminals X, Y and Z of the device. Figure 3.8 shows the first possibility offered by the design of CCII-based transconductors.

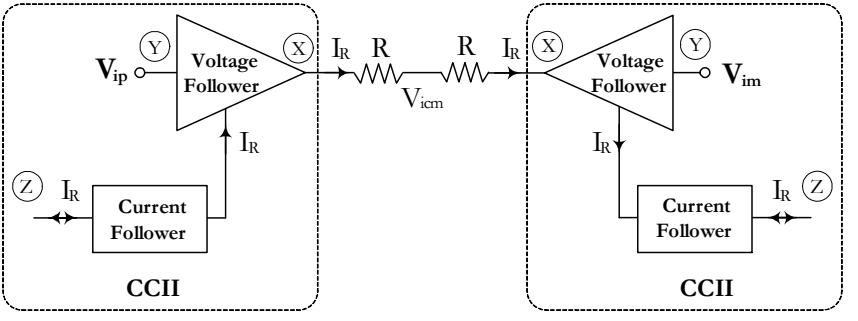

Figure 3.8. CCII-based transconductor with high input resistance

In the first proposal, Figure 3.8, passive resistors are connected between the X terminals of both CCII circuits [7], [8], [26], [30–32]. Due to the fact that

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$V_X = V_Y$, the differential input voltage appears between those terminals and, therefore, the V-I conversion takes place there. Subsequently, the current obtained between the X terminals is driven to the high-impedance output terminals, Z. In this case, the transconductance is equal to

$$G_m = \frac{I_{od}}{V_{id}} = \frac{2I_R}{(V_{ip} - V_{im})} = \frac{2I_R}{V_{id}} = \frac{2(V_{id}/2R)}{V_{id}} = \frac{1}{R} \qquad (3.8)$$

The main advantage of this scheme is its large input resistance. Nevertheless, its main disadvantage is the impossibility of having a rail-to rail input range, as the input signals amplitude range cannot cover from V_{DD} to V_{SS} because the X terminals must track the input voltage.

Assuming balanced inputs, and consequently, complementary voltages at the X terminals, the common terminal of the passive resistors is a signal ground for the differential inputs, which voltage is equal to the common-mode input voltage, V_{icm}. In view of this result, the resistive divider can be employed in order to control the output common-mode voltage of the driving circuit [33].

An alternative implementation based on the previously explained one is represented in Figure 3.9.

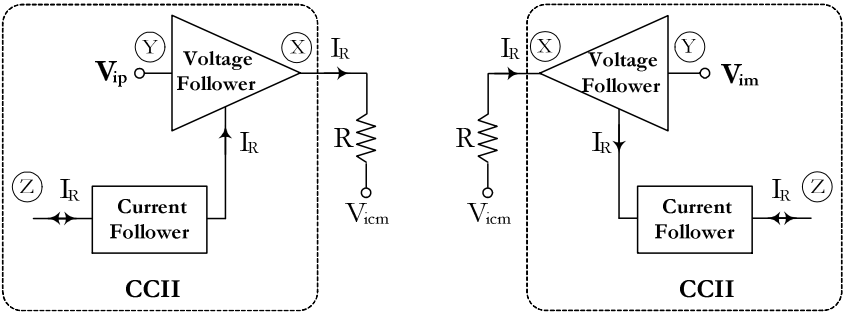

Figure 3.9. CCII-based transconductor: Alternative implementation of Fig. 3.8

In this case, being the transconductor composed of two identical single-ended transconductors, it presents a pseudo-differential topology. This design is viable due to the signal ground seen in the previous implementation. Same as Figure 3.8, this approach also presents some drawbacks. Firstly, mismatch affects this circuit very much because passive resistors must be identical in order to obtain a proper operation of the device. Besides, common-mode input voltage, if

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not constant, must be sensed and applied through a voltage buffer to a signal ground node. Otherwise the Common-Mode Rejection Ratio (CMRR) is not going to have a suitable value.

Another possible implementation of the transconductor is shown in Figure 3.10. In this case the differential input of the transconductor is applied to two matched resistors that are also connected to the X terminals of the CCII circuits [34]. However, the common-mode input voltage is applied this time to the Y terminals but, as $V_X = V_Y$, this voltage is going to appear also at the X terminals. Consequently, the X terminals are going to behave as signal grounds, thus the V-I conversion is going to be very linear. As in the previous cases, the final step lies in driving the current to the high-impedance output. The transconductance of this approach is also the one calculated in expression (3.8).

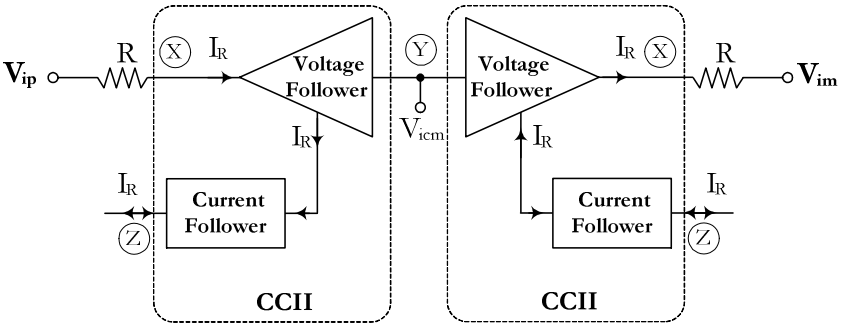

Figure 3.10. CCII-based transconductor with high input range

The advantage of this implementation is that, by using input passive resistors, its input range can be rail-to-rail, unlike the previous designs. However, its input resistance is going to be much lower than in the other proposals and, as a consequence, the circuit providing the signal to the transconductor will end resistively loaded. Moreover, as in the case of Figure 3.9, this design is very sensitive to passive resistors mismatch and the common-mode input voltage still needs to be sensed.

Lastly, another implementation of the transconductor is shown in Figure 3.11. It is based on cross-coupling two transconductors as the ones presented in Figure 3.8 [9], [35]. This configuration is employed with the objective of increasing the linearity. According to the figure, the output current followers are shared between the CCII circuits.

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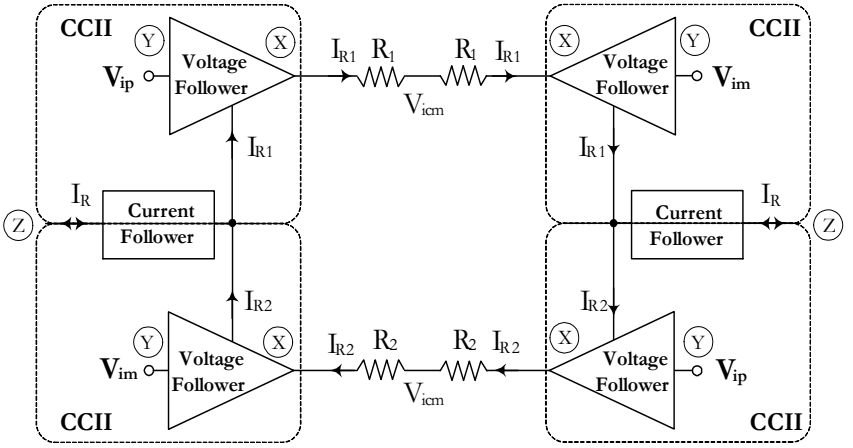

Figure 3.11. CCII-based transconductor using cross-coupled transconductors of Fig. 3.8

The transconductance is different in this case and is obtained from the following expression

$$G_m = \frac{2(I_{R1} - I_{R2})}{(V_{ip} - V_{im})} = \frac{2(I_{R1} - I_{R2})}{V_{id}} = \frac{1}{R_1} - \frac{1}{R_2} \qquad (3.9)$$

This expression proves that low values of transconductance can be achieved without needing to fix large values for R_1 and R_2.

3.4 Design of Class A Voltage Followers

Every transconductor seen in section 3.3 requires CCII circuits in its design, and the first stage of a CCII circuit is a voltage follower. As it has been already mentioned, the voltage follower is in charge of copying the input voltage, applied at terminal Y, to the passive resistor terminal, X, where the V-I conversion is going to take place.

The main requirements for a voltage follower are having high input impedance, low output impedance, and providing an accurate voltage copy between its terminals. It is the duty of the designer to choose the most suitable implementation among the different buffers that fulfill these requirements [1], [36]. All along this section, different choices for the voltage followers are proposed.

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3.4.1 Source Follower (SF)

The source follower or common-drain transistor, the basic single-transistor voltage follower, is the simplest existing implementation and the most widely used one. Source followers are employed as voltage buffers and dc level shifters. Not having a feedback loop in its design, this circuit is characterized by being really fast but not very linear.

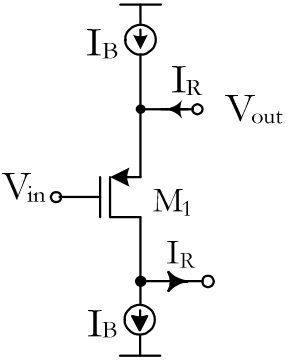

Figure 3.12. Source Follower

According to the figure, the input signal is applied at the high-impedance gate and the output signal, equal to the input signal minus the gate-source voltage V_{GS1}, is obtained at the low-impedance source terminal. The resistor current is sensed at the drain terminal of the input transistor. By using cascode stages, the resistance at the current-sensing node can be increased at the expense of voltage headroom. The main drawback of this topology is its inaccuracy transferring the input voltage to the output terminal due to the dependence presented by the current that goes through the transistor M_1 on the input signal, thus making V_{GS1} also signal dependent. This is unavoidable as two simultaneous tasks are required for transistor M_1: setting the output voltage and driving the load. As a consequence, a small-signal gain appears, as well as a not very low output resistance (typically of a few kΩ):

$$A_v = \frac{V_{out}}{V_{in}} \approx \frac{1}{1 + \frac{g_{mb1}}{g_{m1}} + \frac{1}{g_{m1}R_L}} < 1 \qquad (3.10)$$

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$$r_{out} = \frac{1}{g_{m1} + g_{mb1}} \tag{3.11}$$

being g_{m1} and g_{mb1} the transconductance and backgate transconductance of transistor M_1, respectively. If the transistor is fabricated in an independent well tied to its own source, g_{mb1} does not appear. In order to improve the linearity of the topology and decrease r_{out}, g_{m1} must be increased, thus forcing large bias currents and widths of the transistor which means an increase of area and power dissipation. For that reason it may not be suitable to choose this option in modern very large-scale integration (VLSI) deep-submicrometer CMOS processes with low supply voltages [37].

3.4.2 Flipped Voltage Follower (FVF)

The Flipped Voltage Follower, or FVF, can also be used as a buffer. It is shown in the following figure [38], [39].

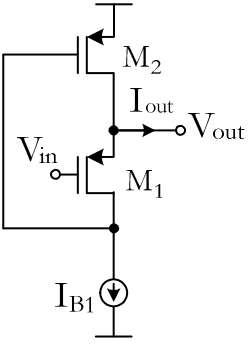

Figure 3.13. Flipped Voltage Follower

Note that this topology makes use of a negative feedback loop, achieved by a second transistor M_2, in charge of driving the load. Due to this addition, transistor M_1 is relieved from that task so that it can be biased with a constant current to optimally set the output voltage, improving linearity and reducing the output resistance, which is now

$$r_{out} = \frac{1}{(g_{m1} + g_{mb1})g_{m2}(r_{o1} || r_{B1})} \tag{3.12}$$

This is typically a few Ohms resistance, in contrast with the one obtained at the SF. Resistance r_{o1} is the drain-source resistance of M_1 and r_{B1} the

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output resistance of the current source I_{B1}. Neglecting channel length modulation and body effect, both current through M_1 and V_{GS1} are constants, improving linearity. As it has been said in the SF section, the body effect can be avoided by embodying M_1 in an independent well connected to its source terminal, causing the disappearance of term g_{mb1} in (3.12) and a reduction of the bandwidth due to the well-substrate capacitance.

Although the FVF is widely used in low-voltage applications, it presents important drawbacks. The main disadvantage of the proposed circuit is that the drain of M_1 is always fixed to the gate voltage of M_2, thus the input voltage range is limited and independent of the supply voltage. The range is given by $|V_{TH1}|$-$|V_{DS1sat}|$, where V_{TH1} and V_{DS1sat} are the threshold voltage and drain-source saturation voltage of transistor M_1. It relies on V_{TH} which is strongly technology-dependent and can be very small in modern deep-submicron processes.

3.4.3 Super Gm

The next voltage follower proposed is known as servo-feedback [26] or super-G_m input stage [7], and it has been widely employed with different implementations of the amplifier.

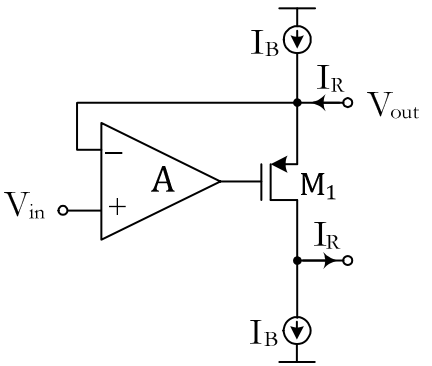

Figure 3.14. Super-Gm Stage

In this case, the accuracy transferring the input voltage to the resistors terminals does not rely on a constant V_{GS} drop in M_1, but on the added feedback loop. Nevertheless, this circuit features some important shortcomings. Its implementation is not simple, at least not as simple as the ones already explained, and compensation is typically required in the amplifier [7]. As a consequence, bandwidth is degraded and power consumption is increased.

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3.4.4 Servo Loop

An alternative configuration, where the implementation of the amplifier can be simpler than in the preceding case, is called servo-loop [26]. This topology is presented in the following figure.

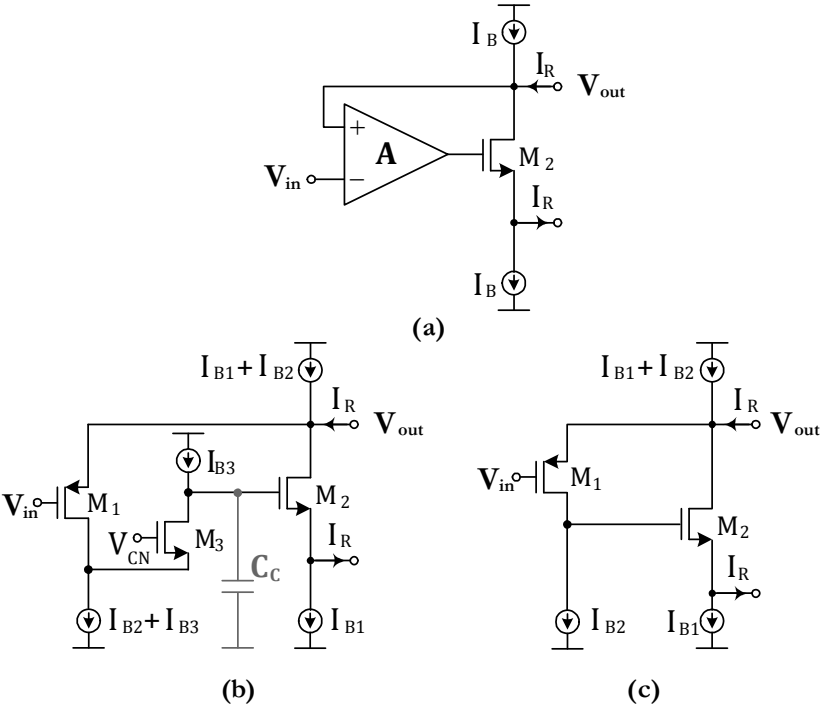

Figure 3.15. (a) Servo-Loop (b) Using folded cascode amplifier (c) Using common-source amplifier.

Figures 3.15 (b) and (c) show two possible implementations of (a), using a folded cascode amplifier [40] and a common-source amplifier, respectively. While case (b) presents additional gain due to its foldind stage, it also suffers an increase of power consumption because of it and requires a compensation capacitor. Among them, the simplest implementation is the one shown in (c). Its simplicity has been achieved by using a single transistor amplifier. This circuit is faster, more power efficient and still provides adequate gain to achieve high linearity. Hence, it is usually chosen over the other configuration. As it will be evidenced later on, this topology is based on the Super Source Follower, SSF,

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being the one presented here more insensitive to mismatch as the current is sensed by a folding stage.

3.4.5 Super Source Follower (SSF)

The SSF, also known as Folded Flipped Voltage Follower (FFVF), is a modification of a voltage follower already explained which is very popular in low-voltage analog design, the Flipped Voltage Follower (FVF). Figure 3.16 shows the configuration of this new proposal [41].

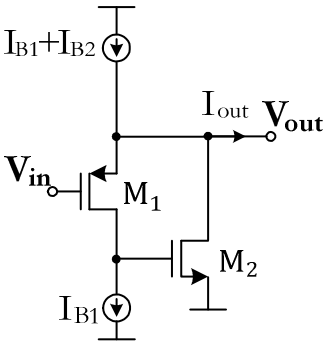

Figure 3.16. Super Source Follower (SSF)

The difference between this topology and the one shown in Figure 3.13 lies in adding the feedback provided by transistor M_2 through an additional branch, seen like a folding of M_2 with respect to the FVF, instead of using a single branch like in the other case. This modification allows overcoming the shortcomings of the FVF configuration. However, both circuits present the same output resistance, given in expression (3.12), and a constant V_{GS1} neglecting second-order effects.

An important difference between the FVF and the FFVF is their input voltage range. In this case is V_{DD}-V_{IB}-$|V_{DS1sat}|$-V_{GS2}-V_{SS}, where V_{IB} is the voltage headroom required for the upper current source to operate ($V_{IB}=|V_{DSsat}|$ if the current source is just a transistor), while the range of the FVF has been specified in section 3.4.2. Note that, opposed to the FVF case where the range is independent of the supply voltage, here it increases with V_{DD}. However, the additional branch that improves the input range increases as well the quiescent power compared with the FVF.

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In summary, the SSF presents some advantageous features in comparison to the other proposed class A voltage followers implementations. For example, it has a higher linearity and much lower output resistance than the SF, and does not have the input range restrictions of the FVF. Nevertheless, like them, it still has an important drawback. Its current driving capability is limited as the maximum current that can be delivered to the load is limited by the bias current. According to the figures shown all along this section, the SF, Super-G_m, Servo-Loop and SSF can sink a large current from the load, but the maximum current they can source is limited to I_B for the SF and Super-G_m configurations and $I_{B1}+I_{B2}$ for the two proposed implementations of Servo-Loop and the SSF. In the FVF, on the contrary, the maximum current that can be sourced to the load is not limited by I_{B1}, but the maximum current sunk from the load is I_{B1}. Obviously, the NMOS versions feature output currents limited by the bias currents in the opposite direction. Consequently, there is a trade-off between quiescent power consumption and slew-rate (SR) performance in all the proposed class A voltage followers topologies.

3.5 Design of Class AB Voltage Followers

In view of the limitations of a class A configuration, a class AB topology seems a better option to implement a voltage follower. In a class A circuit, in order to have good output current signals, large bias currents are needed, with a resulting increase of the quiescent power consumption. Moreover, as it has been already mentioned, a class A operation involves a slew-rate limitation. A class AB operation allows solving these drawbacks without degrading other performance parameters, causing only a small increase in silicon area (typically about 20% in the approach proposed here). Hence, class AB circuits, characterized by their low quiescent power consumption and their high driving capability, are good candidates for low-power analog design.

Class AB operation can be achieved by using QFG techniques, described in the previous chapter [42], [43]. In this case, a class AB topology is derived from a class A one, just by adding a capacitor and a diode-connected MOS transistor operating in cutoff region, which is the implementation of a large-value resistor. Lacking of signal, the performance of the circuit is going to be similar to that of the equivalent class A configuration, shown in section 3.4. However, in dynamic conditions, their performances are going to differ, being the main difference that in class AB the output current is not going to be limited by the quiescent current, so the circuit has the capability to source and sink large

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output currents. This section shows different proposals to implement voltage followers with class AB operation, achieved by QFG techniques or by other methods, highlighting their main advantages and disadvantages.

3.5.1 Class AB FVF

From the FVF implementation, previously shown in Figure 3.13 and widely explained in [38], several class AB implementations can be obtained in order to overcome the drawbacks presented in the classic A topology. The class AB FVF is characterized by a very low output impedance, wide signal range, wide bandwidth, good slew-rate performance and low power dissipation [44], [45].

A first method that allows achieving a class AB FVF is by combining a SF and a FVF, circuits discussed in the previous section [46], [47]. The resulting circuit is able to source and sink a maximum current which is higher than its quiescent current, as expected in a class AB configuration. Figure 3.17 shows this approach.

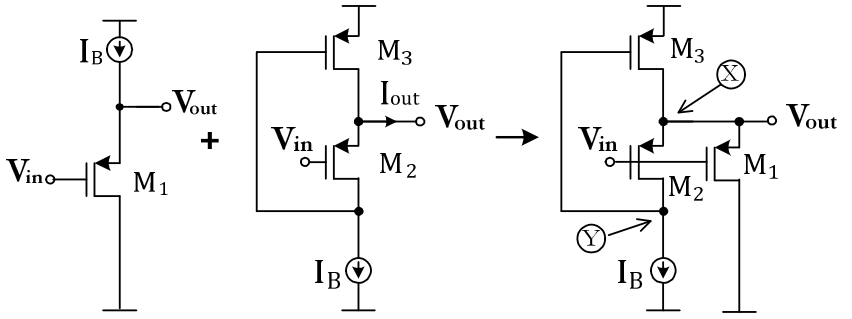

Figure 3.17. Class AB FVF obtained by combining SF and FVF

Assuming a capacitive load for the circuit, under quiescent conditions every transistor is in saturation and no current is delivered to it. The current through M_2 is I_B and, neglecting second-order effects, M_1 copies it as they share the gate and source terminals. Hence, under quiescent conditions, the total current taken from the supply voltage is $2I_B$. However, when for example V_{in} increases with respect to V_{out}, V_{SG} of M_2 tends to decrease and, as M_2 is biased by I_B, its V_{SD} increases, forcing a large current through M_3. Current through M_1 and M_2 is I_B, therefore current though M_3 in excess of $2I_B$ is delivered to the load, increasing V_{out} [47]. This circuit is robust to mismatch and maintains the output voltage constant referred to the input.

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Another possibility to achieve a class AB FVF is by means of QFG techniques, at the expense of small additional hardware and negligible power dissipation. An implementation is proposed in [44]. It is based on a differential FVF, where the input transistor of the FVF has been replaced by a differential pair M_1–M_{1P} and a tail current source. This circuit is characterized by a high range, no attenuation, no DC level shift and output resistance $r_{out} = 1/[g_m(g_m r_o)]$ (~50Ω). This circuit operates in class A and has asymmetrical slew rate (M_{CS} can source large currents into C_L but the maximum negative current in C_L is limited by $2I_B$) until QFG techniques are employed. It requires an additional transistor, M_{AB}, a capacitor and a large resistor, connected as it is shown in Figure 3.18, in order to be transformed into a power efficient class AB circuit.

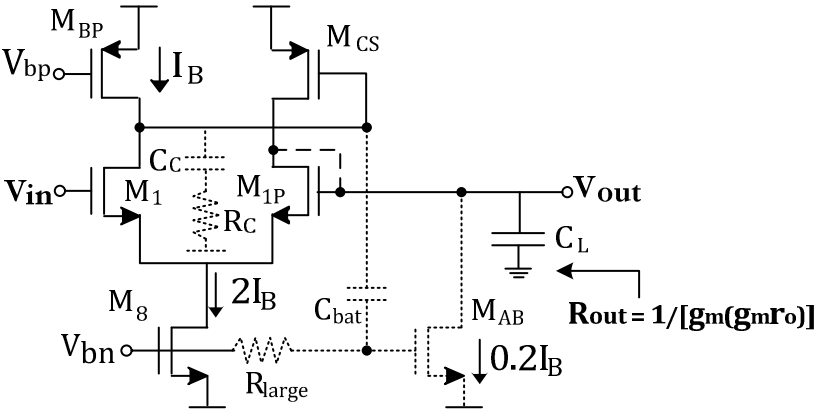

Figure 3.18. Class AB FVF obtained by QFG techniques

Under dynamic conditions, R_{LARGE} prevents flow of charge into the gate of M_{AB}, C_{bat} acts as a floating battery and, as a result, the gate voltage of M_{AB} follows the gate voltage variations of M_{CS}. This is what provides the class AB operation to the proposed buffer. Note that compensation is now necessary. There are more possible implementations of a class AB FVF besides the designs described here. Some examples can be found in papers like [45], [48].

3.5.2 Class AB SSF

Based on the SSF explained before, a class AB version can be obtained [36], [43]. This topology is aimed to solve the slew-rate limitation of class A SSF, providing improved dynamic operation design without degrading other performance parameters. For that reason, it can replace the SSF in virtually any

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circuit proposed to date and it can be regarded as a way to increase the power efficiency of existing SSF-based circuits. By causing only a small increase of silicon area, it preserves quiescent power consumption, accuracy in the quiescent currents, bandwidth, noise level, and supply voltage requirements.

Figure 3.19 shows the class AB implementation of the SSF. This circuit has been achieved by using QFG techniques, reviewed in the previous chapter [42], [43].

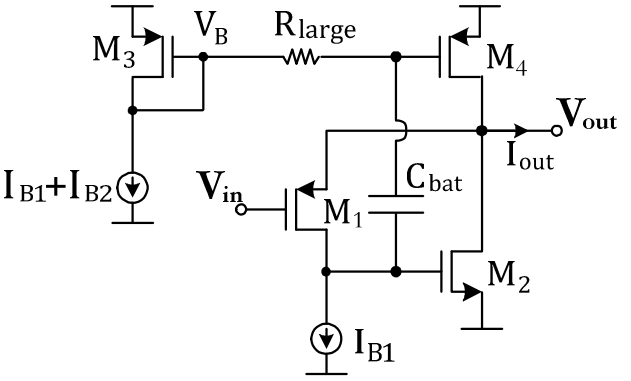

Figure 3.19. Class AB Super Source Follower

According to the figure, the class AB SSF has been achieved just by making the gate of M_4 in the SSF a quasi-floating gate. To do so, as in the FVF proposal, a floating capacitor has been placed between the gates of M_4 and M_2, and a large resistive device between the gate of M_4 and the node that sets the dc bias voltage to V_B.

It must be highlighted that, while class AB operation improves dynamic performance of the device, static behavior is not altered. In quiescent conditions C_{bat} has no effect and there is no voltage drop in resistance R_{large}, hence the quiescent current of M_4 is accurately controlled by the current mirror M_3-M_4, and is supply, process, and temperature independent if I_{B1} and I_{B2} are too, just like the SSF. Therefore, the bias current can be made small to save static power, as it does not limit dynamic currents as opposed to the SSF. In summary, QFG techniques have no impact on static performance.

However, under dynamic conditions, as it has been said before, class AB operation does have a positive effect. Supposing an increase of ΔV_{in} in the input

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voltage, the gate of M_2 is going to suffer a decrease of value $-gm_1ro_1\Delta V_{in}$. This change is going to be translated to the gate of M_4, since the floating capacitor C_{bat} acts as a floating battery and it cannot charge or discharge rapidly. Consequently, V_{SG} of M_4 increases by $\alpha gm_1ro_1\Delta V_{in}$, thus increasing as well its drain current beyond the bias current. Simultaneously, current through M_2 is decreased below its bias current due to its gate voltage drop, contributing in such a way to increase the output current. Similarly, a decrease in the input voltage leads to a current sunk from the load not bounded by the bias current. A detailed analysis of this cell follows, since it is a basic building block in the circuits proposed in this thesis.

3.5.2.1 Small-Signal Analysis

As it has been already mentioned, the static performance of the class AB SSF of Figure 3.19 is identical to that of the conventional SSF of Figure 3.16 hence, for identical device dimensions and bias conditions small-signal device parameters are also identical. Nevertheless, there is one difference in small-signal operation between both circuits, and it lies in the different task carried out by M_4 in both configurations, as it is just a current source in the conventional class A SSF but provides additional transconductance gain at the output stage in the class AB SSF. Using conventional small-signal analysis, the small-signal gain of the class AB SSF results in

$$A_{dc} = \frac{V_{out}}{V_{in}} = \frac{1}{1 + \frac{g_{mb1}}{g_{m1}} + \frac{1}{g_{m1}r_{o1}(g_{m2} + \alpha g_{m4})(r_{o2} || r_{o4})}} \qquad (3.13)$$

and the output resistance is

$$R_{out} \approx \frac{1}{(g_{m1} + g_{mb1})(g_{m2} + \alpha g_{m4})r_{o1}} \qquad (3.14)$$

According to (3.14), R_{out} has been further decreased as compared to the SSF thanks to the new term αg_{m4}, added in the class AB version. Moreover, for the same reason, dc gain is also closer to 1, although this improvement can be unnoticeable if the body effect affects the device and $V_{SB} \neq 0$.

Regarding stability, it must be enforced by doing a proper design. The reason is that, like the conventional SSF, the class AB SSF is a two-pole negative feedback loop. Among them, the dominant pole corresponds to the high-impedance internal node located at the gate of M_2 and is

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$$f_d \approx \frac{1}{2\pi[(g_{m1}+g_{mb1})r_{o1}r_{o2}||\, r_{B1}]C_{G2}} \qquad (3.15)$$

where C_{G2} is the intrinsic capacitance at this node, which is approximately

$$C_{G2} \approx C_{GS2} + C_{Cb} + \frac{C_{bat}C_{GS4}}{C_{bat}+C_{GS4}} \qquad (3.16)$$

with C_{Cb} the bottom-plate to substrate capacitance of C_{bat}. The second pole, the non-dominant one, is located at the output node and is

$$f_{nd} \approx \frac{g_{m1}+g_{mb1}}{2\pi\left(1+\frac{r_{B1}}{r_{o1}}\right)C_L} \qquad (3.17)$$

where C_L is the load capacitance, including the parasitic capacitance at the output node. The open-loop gain of the shunt feedback loop is

$$A_{ol} = -\frac{(g_{m2}+\alpha g_{m4})r_{B1}}{1+\frac{r_{o1}+r_{B1}}{(g_{m1}+g_{mb1})r_{o1}(r_{o2}||r_{o4})}} \approx -(g_{m2}+\alpha g_{m4})r_{B1} \qquad (3.18)$$

In order to enforce stability, f_{nd} should be at least twice the gain-bandwidth product of the loop, i.e., $f_{nd} > 2|A_{ol}|f_d$. From (3.15)-(3.18) this leads to

$$C_L < \frac{1}{2}\frac{g_{m1}+g_{mb1}}{(g_{m2}+\alpha g_{m4})\left(1+\frac{r_{B1}}{r_{o1}}\right)}C_{G2} \qquad (3.19)$$

As for the FVF [39] and SSF topologies, for low load capacitances proper dimensioning of the class AB SSF transistors allows enforcing stability. Note also that, as specified before, if M_1 is embodied in an individual well connected to the source terminal, g_{mb1} does not appear in the above expressions, and the well-to-substrate capacitance of M_1 increases the parasitic capacitance at the output node. As a result, according to (3.19), the maximum value allowed for C_L is reduced in such a case.

If condition (3.19) is not met, then a compensation capacitor connected to the gate of M_2 is needed to increase the capacitance at this node. The value of this compensation capacitor that must be added in order to meet the stability condition mentioned should be:

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$$C_c > 2\left(\frac{g_{m2}+\alpha g_{m4}}{g_{m1}+g_{mb1}}\right)\left(1+\frac{r_{B1}}{r_{o1}}\right)C_L - C_{G2} \qquad (3.20)$$

Another option is using Miller compensation to reduce the value of the C_c required. It should be connected between the gate and drain terminals of M_2.

Finally, the closed-loop bandwidth, if f_{nd} is higher enough than f_d, can be approximated by

$$f_{-3dB} \approx |A_{ol}|f_d \approx -\frac{g_{m2}+\alpha g_{m4}}{2\pi(C_c+C_{G2})}\left[1+\frac{r_{B1}}{(g_{m1}+g_{mb1})r_{o1}r_{o2}}\right] \qquad (3.21)$$

While in the conventional SSF the dominant pole is given also by (3.15), the value of C_{G2} of (3.16) is not the same as the term C_{Cb} does not appear. However, the higher transconductance gain of the output stage in the class AB SSF, which is reflected in the term αg_{m4} in the expressions above, leads to higher open-loop gain as compared to the SSF, leading also to a slightly larger closed-loop bandwidth of the class AB SSF than that of the conventional SSF, as it is shown in Table 3.1. This can be also observed in other QFG output stages [49].

3.5.2.2 Large-Signal Analysis

In a class A SSF, studied in the previous section, $I_{B1}+I_{B2}$ was the maximum current that could be delivered to the load. Consequently, the positive slew-rate was limited to

$$SR_{+,SSF} \approx \frac{I_{B1}+I_{B2}}{C_L} \qquad (3.22)$$

evidencing a tradeoff between SR+ and static power dissipation. Class AB SSF overcomes this problem, as proves the following analytical demonstration based on the approximate MOS square law. In static conditions, the current that goes through M_4 still is $I_4 = I_{B1}+I_{B2}$, fixed by the current mirror, and

$$V_{SG4} = V_{SG4}^{Q} = \sqrt{\frac{2(I_{B1}+I_{B2})}{\beta_4}} + |V_{TH4}| \qquad (3.23)$$

where $\beta_4=\mu_n C_{ox}(W/L)_{M4}$ is the transconductance gain factor of M_4 and the upperscript Q indicates quiescent value.

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Assuming now that a large positive input step V_{step} is applied to the input, M_1 enters cutoff and voltage at the gate of M_2 becomes V_{SS}. As a consequence, M_2 enters cutoff as well and decreases the voltage at the gate of M_4 by $\alpha(V_{G2}^Q+|Vss|)$, leading to the following output current

$$I_{out} \approx I_4 = \frac{\beta_4}{2}\left(V_{SG4}^Q + \alpha V_{G2}^Q + \alpha|V_{SS}| - |V_{TH4}|\right)^2 = \\ = \frac{\beta_4}{2}\left[\sqrt{\frac{2(I_{B1}+I_{B2})}{\beta_4}} + \alpha\left(|V_{SS}| + \sqrt{\frac{2I_{B2}}{\beta_2}} + V_{TH2}\right)\right]^2 \qquad (3.24)$$

which becomes larger than $I_{B1}+I_{B2}$, as expected under dynamic conditions. Hence, the SR+ also increases and becomes larger than the SSF one

$$\frac{SR_{+,AB\ SSF}}{SR_{+,SSF}} = \frac{I_{MAX,AB}}{I_{MAX,A}} \approx \\ \approx \frac{\beta_4}{2(I_{B1}+I_{B2})}\left[\sqrt{\frac{2(I_{B1}+I_{B2})}{\beta_4}} + \alpha\left(|V_{SS}| + \sqrt{\frac{2I_{B2}}{\beta_2}} + V_{TH2}\right)\right]^2 \approx \qquad (3.25) \\ \approx \left[1 + \alpha\sqrt{\frac{\beta_4}{2(I_{B1}+I_{B2})}}\left(|V_{SS}| + \sqrt{\frac{2I_{B2}}{\beta_2}} + V_{TH2}\right)\right]^2$$

Slew rate may be limited in practice to lower values due to the need to drive the gate of M_2 fast enough, particularly if a compensation capacitor is connected to this gate.

Although it is true that class AB operation allows saving quiescent power without degrading dynamic performance by boosting the output current when required, not all class AB topologies are power-efficient. Power efficiency not only implies low static power consumption, but also that most of the power taken from the supplies in dynamic conditions is actually reaching the load. This latter aspect is essential for optimum power management and is quantified by a factor named current utilization [50] or current efficiency (CE) and is defined as the ratio of the load current to the supply current, i.e., CE=Iout/Isupply. For a class AB SSF is approximately given by

$$CE = \frac{|I_{out}|}{|I_{out}| + I_{B1} + I_{B2}} = \frac{1}{1 + \frac{I_{B1}+I_{B2}}{|I_{out}|}} \qquad (3.26)$$

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Under dynamic conditions current efficiency approaches the ideal value of 1 since $|I_{out}| >> I_{B1}+I_{B2}$ also for $V_{in} > 0$. The reason for obtaining such a high CE value is that in the class AB SSF, as opposed to other class AB topologies, the large dynamic currents are generated directly in the output transistors, without internal replication, avoiding that way losses that take place while replicating the current that cause a CE drop below 0.5 [50].

3.5.2.3 Second-Order Effects and Noise Analysis

While designing a circuit, it must be taken into account that temperature and supply voltage variations, and geometric and parametric mismatches may occur. A class AB SSF allows well controlled quiescent currents regardless of supply or temperature variations due to the current mirroring employed to obtain them. So, if I_{B1} and I_{B2} are independent of these variations, quiescent currents are too. Nevertheless, quiescent currents are going to be affected by mismatches either in transistors M_3 and M_4 or in the transistors implementing the current sources. The way the currents are affected is exactly the same as for the conventional SSF, meaning that the class AB version does not make this cell more sensitive to mismatch, process, or temperature variations. To obtain the class AB operation just a resistor and a capacitor have been added, and variations in their value due to process or temperature changes do not affect static performance, they just modify the cutoff frequency, which is not relevant as long as the resulting frequency remains below the minimum frequency component of the signal.

However, absolute process variations do affect dynamic operation, e.g. the maximum output current in (3.24) which is dependent on the threshold voltage and transconductance factor and, consequently, the SR+. According to this, process tolerances must be considered at the design stage in order to reach the proper performance of the circuit, even if obtaining the exact maximum values is not necessary as long as they are high enough to achieve a given settling performance.

Another issue that deserves consideration is the body or bulk effect, due to the influence of the bulk voltage on the MOSFET inversion layer. It is usually modeled as an increase in the absolute value of the threshold voltage given by

$$V_{TH} = V_{TH0} + \gamma\left|\sqrt{\varphi_F + V_{SB}} - \sqrt{\varphi_F}\right| \qquad (3.27)$$

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where all the terms have their usual meaning [51]. This variation can also be reflected in an additional small-signal transconductance term given by $g_{mb}v_{sb}$, but only if source and bulk terminals are not connected. Hence in the class AB SSF only M_1 may suffer this effect, if it is not embodied in an individual well connected to the source terminal. In the small-signal analysis we have seen this effect reflected in the g_{mb1} term. On the other hand, in large-signal operation it makes the dc level shift between input and output terminals dependent on the input signal, degrading linearity, but only again unless an individual n-well is used for M_1. However, in this case, the additional source-to-substrate nonlinear capacitance increases parasitic capacitance at the output node and distortion, and should only be considered when compensation is employed.

Concerning noise, the main sources in CMOS analog circuits are thermal and flicker noise. Considering thermal noise and assuming as usual that noise sources are uncorrelated, the approximate expression for the equivalent input noise density of the class AB SSF is

$$\overline{v_{N,in}^2(f)} \approx \frac{8}{3}k_B T \left\{ \begin{array}{l} \dfrac{1}{g_{m1}} + \dfrac{1}{g_{m2}g_{m1}^2(r_{B1}||r_{o1})^2} + \\ + \dfrac{g_{m4}}{[g_{m1}(g_{m2}+\alpha g_{m4})(r_{B1}||r_{o1})]^2} + \dfrac{g_{mB1}}{g_{m1}^2} \end{array} \right\} \qquad (3.28)$$

where k_B is the Boltzmann's constant and T the absolute temperature. Parameters g_{mB1} and r_{B1} are the transconductance and output resistance, respectively, of current source I_{B1}. According to the expression, the equivalent input noise is dominated by the thermal noise of the input transistor and the current source I_{B1}. Both noise contributions are reduced by increasing g_{m1}.

Concerning flicker noise and assuming again uncorrelated noise sources the equivalent input noise density becomes

$$\overline{v_{N,in}^2(f)} \approx \frac{1}{C_{ox}f} \left\{ \begin{array}{l} \dfrac{K_1}{W_1L_1} + \dfrac{1}{g_{m1}^2(r_{B1}||r_{o1})^2}\dfrac{K_2}{W_2L_2} + \\ + \dfrac{1+I_{B2}/I_{B1}}{(g_{m2}+\alpha g_{m4})^2(r_{B1}||r_{o1})^2}\dfrac{K_4L_1}{W_1L_4^2} + \dfrac{\mu_n}{\mu_p}\dfrac{K_{B1}L_1}{W_1L_{B1}^2} \end{array} \right\} \qquad (3.29)$$

where the constant K_i is dependent on transistor M_i and can vary widely for different devices in the same process. C_{ox} is the capacitance per unit area, W_i and L_i the width and length of M_i, and μ_n and μ_p are the mobility of electrons and holes, respectively. As for the thermal noise, the main noise contribution is due to M_1 and the transistor, with aspect ratio W_{B1}/L_{B1}, which implements the current

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source I_{B1}. For $L_1=L_{B1}$, and noting that $\mu_n>\mu_p$ and $K_{B1}>K_1$ (as NMOS transistors usually have larger flicker noise than PMOS transistors), flicker noise is dominated by I_{B1}. Taking L_{B1} longer greatly reduces the input-referred flicker noise, but it increases the minimum voltage required in I_{B1} to operate in saturation. Besides, taking W_1 larger decreases both the input-referred flicker noise and the thermal noise, as shown in (3.28) and (3.29), and from (3.17) it also increases the frequency of the non-dominant pole.

Both class A and class AB SSF feature essentially the same input noise density as they have equal dominant noise terms given by the input transistor and the current source I_{B1} in their aforementioned noise expressions. However, although they do not influence the dominant terms, the equivalent input noise of a class A SSF has some modifications in relation to (3.28) and (3.29), the term αg_{m4} disappears and there is an additional term due to the noise of M_3. Other techniques that allow achieving class AB operation do not have this advantage, as they may require additional circuitry that may increase noise level.

3.5.2.4 Experimental Results

This section is focused on showing different measurement results of some explained voltage followers and comparing them. All of them were fabricated in a 0.5-µm CMOS n-well process with nominal NMOS and PMOS threshold voltages of 0.67 V and –0.96 V, respectively. Regarding class AB components, capacitor C_{bat} was a poly-poly capacitor of 1 pF and resistance R_{large} was implemented by a diode-connected PMOS transistor of W/L=1.5/1. High-swing cascode current sources were employed. Transistor dimensions W/L (in µm/µm) were 72/0.6 (M_1), 60/1 (M_2), and 200/1 (M_3, M_4). The supply voltages employed for all the measurements were V_{DD}=1.65 V and V_{SS}= -1.65 V. The bias currents were $I_{B1}=I_{B2}$=10 µA. Finally, a large load capacitance was employed ($C_L\approx$50 pF), which includes the pad, board and test probe capacitance, in order to prove the class AB driving capability of the class AB SSF when measured.

Figure 3.20 includes in its microphotograph the design of three voltage followers, which cannot be separately identified as they are highly interdigitized, the SF, the SSF and the widely analyzed class AB SSF. The silicon area employed is 5000 µm² for the SF, 7200 µm² for the SSF and 8700 µm² for the class AB SSF, i.e. a 20% area increase regarding class A version.

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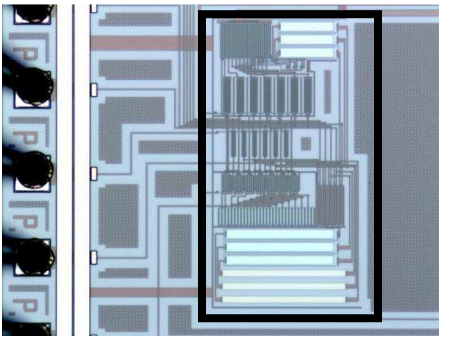

Figure 3.20. Microphotograph of the voltage followers

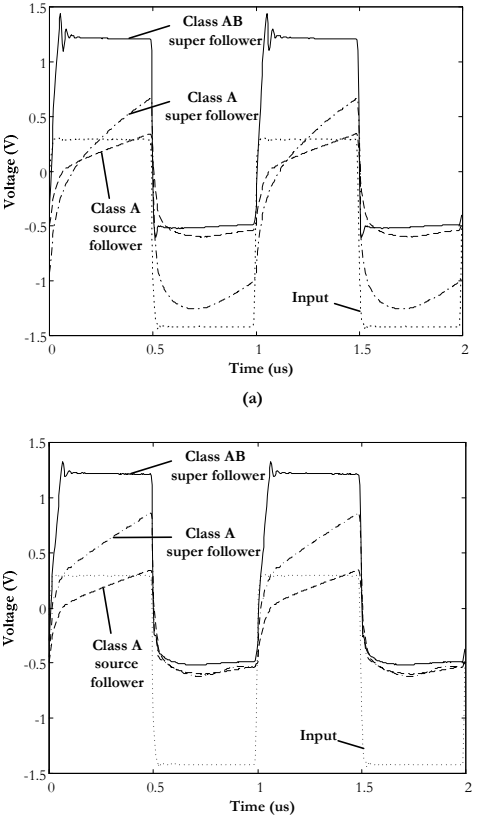

Figure 3.21. Measured response to an input square waveform
(a) Uncompensated followers (b) Compensated followers

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The first measurement, shown in Figure 3.21 (a), is the response of the three followers to a 1 MHz periodic input square waveform with peak-to-peak amplitude of 1.8 V and dc level of -0.6 V. As it has been said in previous explanations and can be clearly seen in the figure, class A SF and SSF have limited positive slew-rate. Consequently, they are unable to track the input voltage. However, according to the discussion, class AB SSF features a much larger positive slew rate not limited by the bias current that makes it capable of tracking the input almost perfectly. In fact, from (3.26) its measured maximum CE charging the load capacitor is approximately 0.99, while the theoretical one for the SSF is only 0.5. However, figure shows a degraded settling performance due to this large load capacitance value.

Trying to improve the response of the followers, another version of the class A and class AB SSF was fabricated in the same chip using a Miller compensation capacitor of 1.8 pF, in series with a nulling resistor of 20 kΩ, between the gate of M_2 and the output node to split the dominant and non-dominant poles. Figure 3.21 (b) shows the measured transient response of the compensated SSF, for the same input waveform as before. Note that ringing in class AB SSF is reduced at the expense of a decrease in slew rate, evidencing that slew rate is limited by the ability to drive the compensation capacitor in this case. Besides, CE slightly decreases to 0.98. Nevertheless, compensation is not required for small capacitive loads, like those normally employed on-chip, according to (3.19).

Main measured performance parameters of the voltage followers, uncompensated and compensated versions, are summarized in Table 3.1.

Table 3.1. Measured performance of the voltage followers

Parameter	SF	SSF	Compensat. SSF	Class AB SSF	Compensat. class AB SSF
SR+	0.8 V/µs	1.9 V/µs	1.3 V/µs	41 V/µs	24 V/µs
SR-	-23 V/µs	-130 V/µs	-114 V/µs	-135 V/µs	-119 V/µs
THD @ 1Vpp, 100kHz	>-10dB	>-10dB	>-10dB	-57 dB	-57 dB
Bandwidth	0.7MHz	12MHz	5MHz	13.1MHz	8MHz
Eq. input noise @1MHz	13nV/√Hz	12nV/√Hz	12 nV/√Hz	12 nV/√Hz	12 nV/√Hz
Power	33 µW	66 µW	66 µW	66 µW	66 µW
Silicon area	5000 µm²	7200 µm²	9200 µm²	8700 µm²	10700 µm²

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As expected, SR+ of class AB SSF is larger than in other topologies, especially on the uncompensated version. It shows an increase factor of 21.5 for the uncompensated version and of 18.5 for the compensated one as compared with the conventional class A SSF. Moreover, its Total Harmonic Distortion (THD) is -57dB for an input voltage of 1Vpp, much lower than in other configurations incapables of tracking the input waveform due to their positive slew-rate limitation that leads to a strongly distorted output waveform. An illustration of this issue is found in Figure 3.22. The dominant distortion term, the second order one, can be notably reduced using a differential configuration.

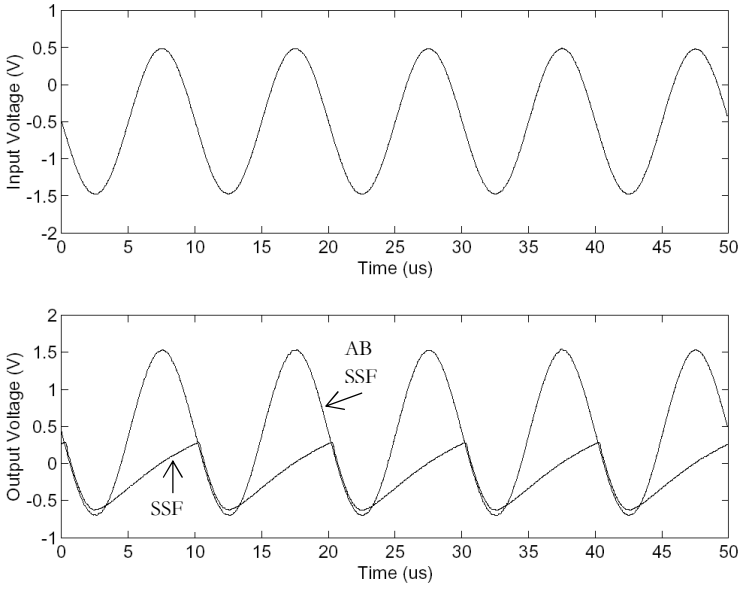

Figure 3.22. Measured response to a 100 kHz input sinusoid
(a) Input Voltage (b) Output voltage of class A and class AB SSF

3.5.3 Other Class AB Buffers based on the SSF

Other class AB buffer proposals can be obtained from the SSF. The advantages of the SSF configuration will remain in the new topologies, but they also will include in their design some useful new features, making them the suitable circuit for a particular application. Obviously, these new circuits will try also to overcome the drawbacks of the SSF.

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3.5.3.1 Differential Class AB Buffer

As mentioned before, a differential configuration allows reducing the high second order distortion, which is the dominant term in a class AB SSF and the cause of its limited linearity. Moreover, it allows alleviating as well another shortcoming of the class AB SSF, its input-output dc level shift equal to the V_{SG} of transistor M_1 [52], [53], which is process and technology dependent. Figure 3.23 shows the proposed differential topology [36].

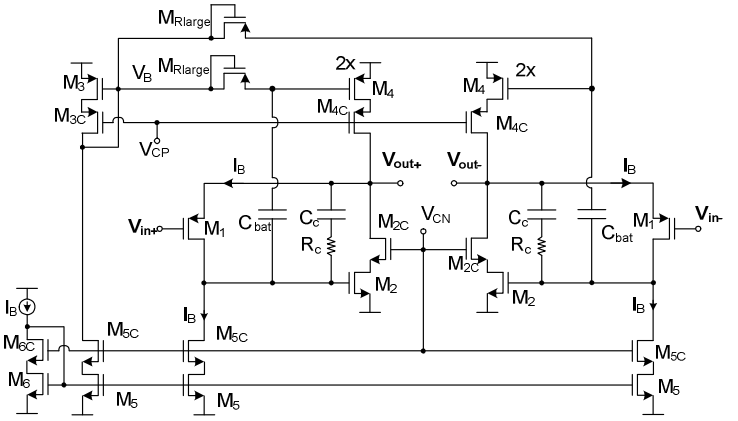

Figure 3.23. Differential Class AB SSF

There are a few differences between this version and the single-ended one, although transistor dimensions and capacitor values are the same.

Table 3.2. Measured performance of the Differential class AB SSF

Parameter	Value
Technology	0.5-μm CMOS
Supply voltages	±1.65V
Bias current I_B	10 μA
THD @ 100Hz, 1Vpp	-69 dB
Bandwidth	8 MHz
Equivalent input noise @ 3MHz	28 nV/√Hz
CMRR @ 100kHz	62 dB
Quiescent power consumption	132 μW
Silicon area	0.02 mm²

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Some cascode transistors have been included in this new version, like M_{2C} and M_{4C}, to increase the loop gain and to improve the accuracy copying the quiescent currents, respectively. Besides, compensation was needed in order to drive large off-chip capacitive loads. Its layout can be found also in Figure 3.20, where the total area it employs is 0.02 mm^2. Table 3.2 shows the main performance parameters obtained using the same supply, load, and bias currents as for the single-ended buffers.

3.5.3.2 Two-stage Class AB Buffers

Another possibility consists in designing two-stage class AB voltage followers. A systematic approach for this is proposed in [54], based on the inclusion of a class AB operation to class A Miller amplifier topologies in unity-gain negative feedback by a simple technique that does not modify quiescent currents, supply requirements, noise performance, or static power. The technique, aimed to systematically derive two-stage class AB unity-gain buffers from class A implementations, lies in using QFG techniques [42], [49], [55]. The following figure illustrates the basic design principle. According to it, just by adding the QFG components, C_{bat} and R_{large}, a generic class A buffer formed by a two-stage Miller amplifier in unity-gain negative feedback is transformed into its class AB version.

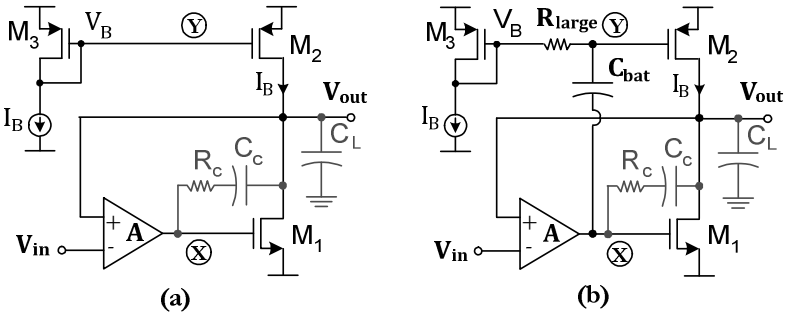

Figure 3.24. (a) Two-stage class A buffer (b) Two-stage class AB buffer

In both cases, amplifier A is a generic single-stage amplifier with dc gain $A=G_{mA}R_A$, where G_{mA} and R_A are its transconductance and output resistance. Amplifier A together with transistor M_1 form a negative feedback loop with a high dc loop gain of $A_{ol}=G_{mA}R_A g_{m1}(r_{o1}||r_{o2})$, where g_{mi} and r_{oi} are the transconductance and output resistance of transistor M_i, respectively. This high loop gain forces the output voltage to track the input voltage and, consequently, the dc closed-loop gain of the buffer is

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$$A_{cl} = \frac{V_{out}}{V_{in}} = \frac{A_{ol}}{1 + A_{ol}} \approx 1 \qquad (3.30)$$

Also due to the feedback loop the low output resistance is

$$R_{out} = \frac{1}{G_{mA} R_A g_{m1}} \qquad (3.31)$$

Stability of the feedback loop in Figure 3.24(a) is enforced by creating a dominant pole f_{p1} at node X using Miller compensation, while the non-dominant pole f_{p2} corresponds to the output node. However, even though high accuracy and low output resistance have been achieved in the circuit of Figure 3.24(a), the maximum current that can be delivered to the load is limited by I_B, limiting in turn its positive slew rate (supposing amplifier A has enough driving capability in order not to additionally limit slewing).

This drawback, inherent in class A topologies, has been overcome in Figure 3.24(b), as it can be avoided by obtaining class AB operation. By employing QFG techniques, the voltage follower gain increases and the output resistance and dominant pole frequency decrease. Note, however, that the product $GB=A_{ol}f_{p1}$ remains the same as in the class A follower.

The two-stage class AB buffer proposed in Figure 3.24(b) can be regarded as an extension of the topology reported in [43], replacing the input transistor by a generic input stage (amplifier A) and its principle of operation is similar to that of a conventional class-AB two-stage OTA. Several class AB buffers can be obtained by using different implementations for amplifier A. Three possible realizations are shown in Figure 3.25.

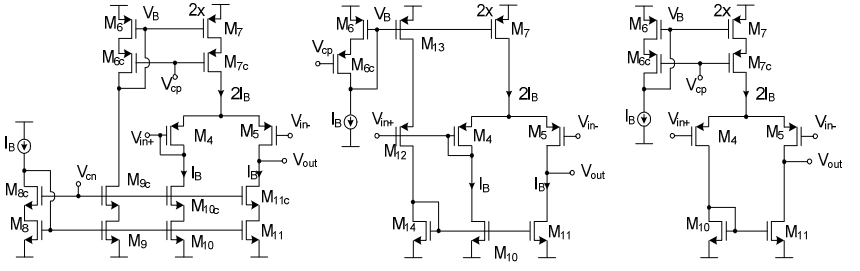

Figure 3.25. Basic amplifiers (a) With dc level compensation (b) Alternative realization (c) Differential pair

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The proposal 3.25(a) shows a basic amplifier where gain is provided by transistor M_5. Matched diode-connected transistor M_4, biased with the same current, has been included in order to compensate for the DC level shift V_{GS5} that takes place in M_5 and that otherwise would appear between the amplifier inputs. Such DC level shift depends on process and temperature variations, and also on the bulk effect if M_5 is not embodied in a well tied to its source terminal. In this case, both M_4 and M_5 have been embodied in a common well tied to the common source terminal, thus avoiding the body effect, and the resulting DC gain of this amplifier is $A \approx g_{m5} r_{o5}$. The amplifier of Figure 3.25(b), that employs an alternative biasing based on the one of circuit (a), tolerates a larger input common mode range. For this reason, cascode current sources have been eliminated, and transistor M_{12} (matched with M_4 and M_5) has been included to preserve accuracy. By providing the same V_{DS} as M_{13} and M_7, even when they enter triode region, the current across M_{13} and M_{14} will still be exactly half that of M_7, thus yielding accurate voltage copy between the buffer input and output. The DC gain of this proposal is $A \approx g_{m5}(r_{o5} \| r_{o11})$. Finally, Figure 3.25(c) presents a conventional differential pair and its DC gain is also $A \approx g_{m5}(r_{o5} \| r_{o11})$.

After being fabricated in a 0.5 μm CMOS process [54], measurements demonstrate a notable improvement of dynamic performance with a minor penalty in terms of silicon area comparing them with their class A counterparts. In particular, the slew rate improvement factor is nearly 100. These results make these buffers suitable for systems requiring accurate operation with very low quiescent power consumption.

3.6 Design of Class A Current Followers

As mentioned at the beginning of this chapter, after the voltage follower and the passive resistors in charge of the V-I conversion, a current follower is usually employed in order to set a proper DC input voltage and convey the sensed current, taken at a low-impedance input, to a high-impedance output terminal. In this way, the current follower allows improving the output resistance and maximizing the output voltage swing. Thus, they require very low input impedance with well-controlled dc voltage, very high output impedance, and current compliance. Several circuits can be chosen for this task, and some of their implementations are proposed in this section [56].

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3.6.1 Current Mirrors

Although there are many implementations for this simple circuit, Figure 3.26 shows a possible current mirror realization [57].

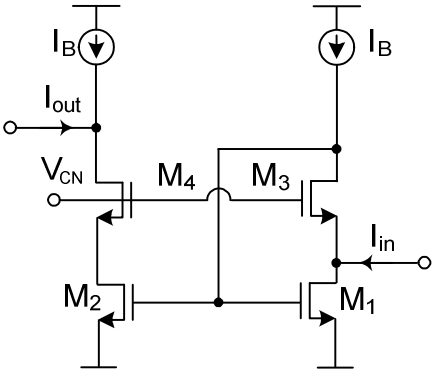

Figure 3.26. Current Mirror

This is a widely used approach and is simple, but it requires matching in the current mirror transistors and two branches with signal currents, increasing power consumption. This is a problem if the design strategy shown in Figure 3.7(b) is employed, as it is strongly insensitive to device mismatch since it relies on high-gain feedback loops and a passive component, and its insensitivity is lost if a current mirror is included in its design.

Moreover, when the node of the voltage follower where the resistor current is sensed corresponds to a source terminal, e.g. Servo-Loop configuration, this sensing node can be grounded and the output transistor becomes the input stage of the current mirror. Hence in this case the input stage of the current mirror provides gain to the feedback loop of the voltage follower and simultaneously senses the input current. This idea is used in [26], [34], [58].

3.6.2 Folding Stage

A second alternative for the task is using a Folding Stage as a current follower [35]. It is the simplest yet efficient mismatch-insensitive current buffer. Its design is shown in Figure 3.27. Unfortunately, this approach features a not very low input resistance and a not very high output resistance.

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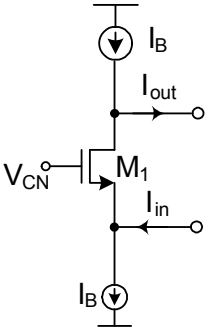

Figure 3.27. Folding Stage

3.6.3 Regulated Cascode Stage

Figure 3.28 illustrates a regulated cascode stage, another possibility for implementing a current follower [7], [31]. Although this circuit features lower input resistance, higher output resistance, and is also mismatch-insensitive, it has two main disadvantages which are the reduction of the voltage swing at the output stage due to the stacked V_{GS} voltages, and the reduction of the input swing in the transconductor. Besides, this circuit requires additional quiescent power consumption. Being those important drawbacks for a low-power system, it is not the most chosen topology.

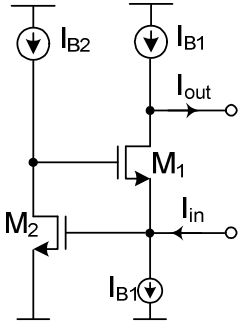

Figure 3.28. Regulated cascode stage

3.6.4 FGMOS Regulated Cascode Stage

The disadvantages of the regulated cascode stage just described can be overcome by using an alternative implementation shown in Figure 3.29. In this

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case, M_2 is a two-input FGMOS transistor, and the capacitive division allows decreasing the input voltage V_{bias}.

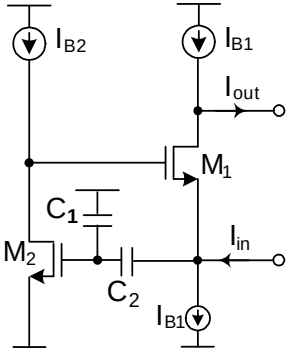

Figure 3.29. FGMOS regulated cascode stage

The gate voltage of M_2, assuming that C_1 and C_2 are much larger than the parasitic capacitances, is

$$V_{G2} = \frac{C_1}{C_1 + C_2} V_{DD} + \frac{C_2}{C_1 + C_2} V_{bias} \qquad (3.32)$$

Rearranging the terms, V_{bias} becomes

$$V_{bias} = \left(1 + \frac{C_2}{C_1}\right) V_{G2} - \frac{C_2}{C_1} V_{DD} \qquad (3.33)$$

where

$$V_{G2} = V_{SS} + V_{GS2} = V_{SS} + V_{TH2} + \sqrt{\frac{2I_{B2}}{\mu_n C_{ox} (W/L)_{M2}}} \qquad (3.34)$$

having all the terms their usual meaning. Thus, V_{bias} can be adjusted by the ratio C_2/C_1, and can be set to the minimum value required. This is how the input voltage of the follower is decreased, and therefore the minimum input and output voltage of the transconductor, in a transistor's threshold voltage.

3.7 Design of Class AB Current Followers

Once a class AB voltage follower has been implemented, it is convenient to use also a class AB current follower to implement the transconductor.

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Otherwise, the advantages achieved by employing class AB operation in other parts of the circuit, are going to be lost when a class A current follower is included in the design.

Once again, class AB operation can be achieved by using QFG techniques, aimed to modify a class A circuit in order to make it more power-efficient and suitable for low-power consumption systems. Very popular and widely employed current followers are class AB current mirrors, described in the following section [36].

3.7.1 Class AB Current Mirrors

As an application of the class AB SSF, a class AB current mirror can be easily obtained, as it is shown in Figure 3.30 (a). The input current is sensed by the class AB SSF, and copied to a high-impedance output terminal by replicating transistors M_2 and M_4. Input voltage is set by the dc voltage V_{bias} and bias current I_{B1}, and is given by

$$V_{in} = V_{bias} + V_{SG1} = V_{bias} + |V_{TH1}| + \sqrt{\frac{2I_{B1}}{\beta_1}} \qquad (3.35)$$

Dc level shift V_{SG1} is temperature and process dependent, resulting in an inaccurate setting of the input voltage. However, in most applications the sensing node does not require a very precise dc value. If this is not the case, a diode-connected transistor matched with M_1 can be employed [59] to compensate it, or a fully differential version can be employed.

The input resistance corresponds to (3.14). Due to the use of the QFG technique the input and output currents can be much larger than the quiescent currents, which are accurately set to I_{B2} in the input and output branches. Note that a class AB current amplifier with gain K can also be obtained by choosing the W/L of M_{2M} and M_{4M} K times larger than that of M_2 and M_4.

To improve the accuracy of the current copy and to increase output resistance, transistors of Figure 3.30 (a) should be cascoded. This has been already done in the differential class AB current mirror of Figure 3.30 (b), where $I_{B1}=I_{B2}=I_B$. This circuit has been fabricated and measured.

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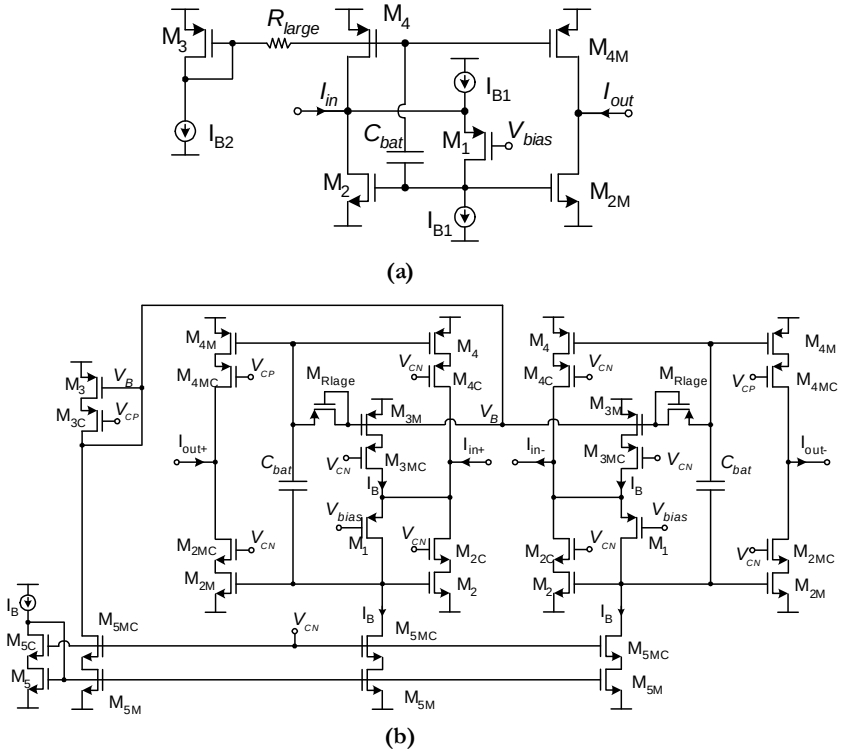

Figure 3.30. Class AB current mirror (a) Basic idea (b) Differential version

Measurements carried out for a supply voltage of ±1.65V and bias current I_{B1}=I_{B2}=10μA shows a THD of -62 dB for an input current of 100 kHz and 200μApp, i.e., 20 times larger than the bias current, reflecting the proper class AB operation. Power consumption is 264μW, and the silicon area employed is 0.035 mm².

3.8 Design of Class AB Current Conveyors

To make a second generation current conveyor (CCII) an attractive design option for the currently dominant applications, CCIIs should be designed in CMOS technologies and operate with low supply voltage and low power consumption. By achieving class AB operation its performance is going to improve, becoming more suitable for this kind of applications. The input and output currents of the CCII are not going to be limited by the bias currents, and

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therefore low quiescent power consumption and high dynamic current driving capability can be achieved simultaneously.

Several ways of obtaining class AB operation for a CMOS CCII can be found in literature [60–62]. A conventional class AB CMOS CCII is discussed in [63] and shown in Figure 3.31.

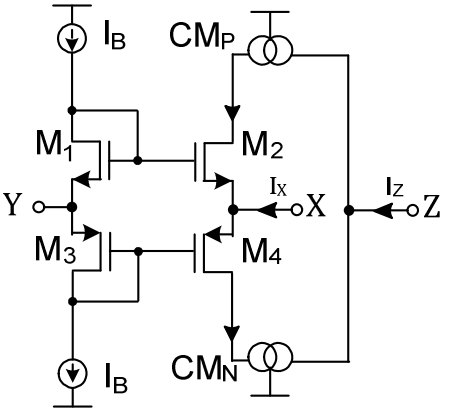

Figure 3.31. Conventional Class AB CCII

In this circuit, class AB operation is achieved by the dc level shift implemented by the diode-connected transistors M_1 and M_3, which sets the quiescent current in transistors M_2-M_4 but increases supply requirements and requires additional quiescent power consumption. Moreover, this circuit has serious drawbacks, like the possibility of having a tracking error between V_Y and V_X if there is a resistive load in terminal X, or a not too small small-signal output resistance also in X, or its sensitivity to transistor mismatch [29].

Other topologies of class AB CCII can be implemented in order to overcome the mentioned drawbacks. In these new proposals class AB operation is obtained without extra supply voltage or quiescent power requirements, using Quasi-Floating Gate techniques [25], [29]. Besides, a local feedback loop can be employed to decrease drastically input resistance at node X. A realization of a class AB CCII based on QFG techniques is illustrated in Figure 3.32 [25]. Note that this is basically the class AB current mirror of Fig. 3.30(a) employed as CCII, or the class AB SSF with replicated output branch.

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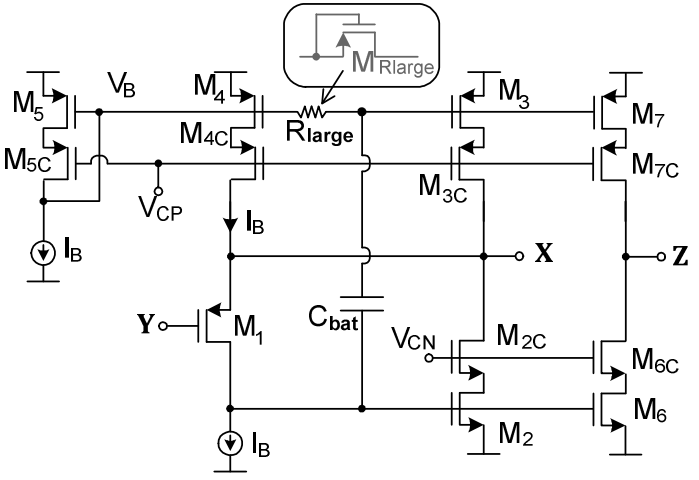

Figure 3.32. Class AB CCII based on QFG techniques

According to the figure, a voltage follower replicates voltage from terminal Y to terminal X. It is made by the source follower transistor M_1 and transistors M_2-M_{2C} which provide negative feedback. Transistor M_1 carries a constant current I_B, which neglecting second-order effects leads to a constant source-to-gate voltage V_{SG1}. This feature improves linearity as compared to the conventional source follower. Transistor M_3 is a Quasi-Floating Gate (QFG) transistor and provides class AB operation. This transistor has a stable DC bias voltage set through a large valued resistive device R_{large}, and a signal voltage coupled by a floating capacitor C_{bat}.

As it has been explained in the QFG techniques section, the quiescent current of M_3 is accurately controlled by the current mirror M_3-M_5, and is supply, process, and temperature independent. This static current can be made small to save static power. Hence R_{large} and C_{bat} do not modify static performance. However, dynamic performance is improved as the gate voltage of M3 becomes signal-dependent, providing extra output transconductance and allowing class AB operation. For instance, as it has been mentioned before, an increase Δvin in the input voltage leads to a decrease at the gate of M_2 of value $-g_{m1}r_{o1}\Delta$vin which is propagated at the gate of M_3 since the floating capacitor C_{bat} acts as a floating battery. Hence the V_{SG} of M_3 increases by $\alpha g_{m1}r_{o1}\Delta$vin, where $\alpha=C_{bat}/(C_{bat}+C_{G3})$ is the attenuation from the gate of M_2 to the gate of M_3, and C_{G3} is the parasitic capacitance at the gate of M_3. This increment in V_{SG3} increases the drain current of M_3 beyond the bias current. At the same time the voltage drop at the

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gate of M_2 also decreases current in M_2 below its bias current, thus also contributing to increase the output current at terminal X. In a similar way a decrease in the input voltage leads to a current sunk from terminal X not bounded by the bias current. This current is replicated to the high-impedance output terminal Z by cascode current mirrors.

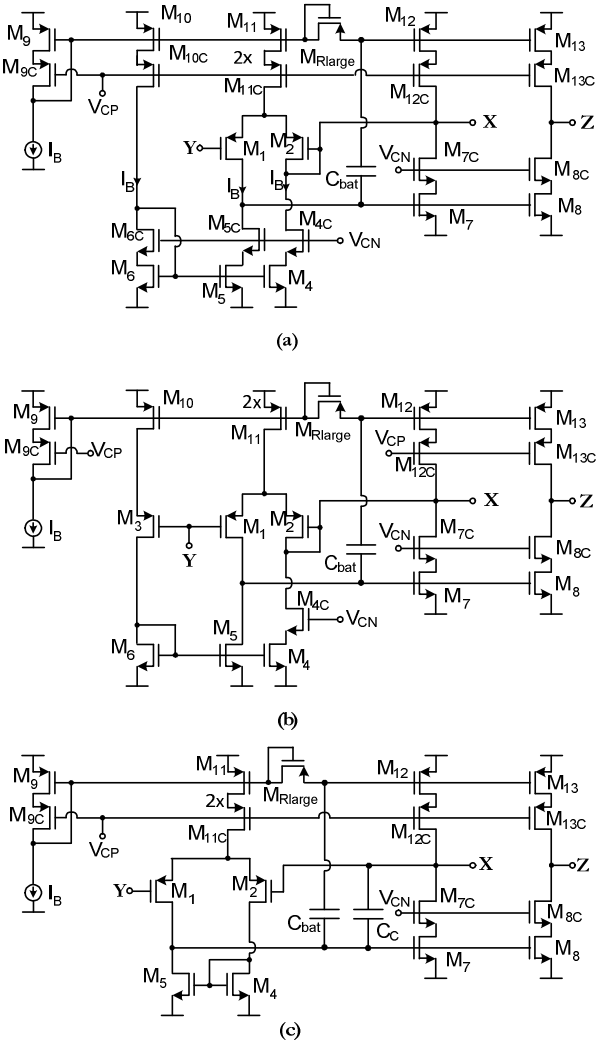

Figure 3.33. Class AB CCIIs (a)With DC compensation (b) DC compensation and increased input range (c) With differential pair

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A RC high-pass filtering occurs between the gates of M_2 and M_3, which is given by:

$$\frac{V_{G3}(s)}{V_{G2}(s)} = \alpha \frac{sR_{large}(C_{bat} + C_{G3})}{sR_{large}(C_{bat} + C_{G3}) + 1} \qquad (3.36)$$

R_{large} does not require to be linear or to have a precise value, but it should be high enough to provide a cutoff frequency $f_{-3dB}=1/[2\pi R_{large}(C_{bat}+C_{G3})]$ lower than the minimum frequency component of the input signal. In baseband applications usually only the DC component should be blocked. Due to the mentioned tolerance to the exact value or R_{large}, process, voltage, or temperature variations affecting this resistance are not relevant and it can be implemented by the leakage resistance of a minimum-size diode-connected MOS transistor in cutoff region, not demanding extra power consumption.

By slightly modifying the circuit of Figure 3.32, some alternatives of class AB CCII circuits are obtained and presented in Figure 3.33 [64]. The proposal of Figure 3.33 (a) includes a matched diode-connected transistor M_2 biased by the same current I_B, in order to cancel out the DC level shift equal to the V_{SG} of M_1 that appears in Figure 3.32 between Y and X terminals. This shift can also be eliminated by using a differential configuration of the circuit, without doing any alteration. Approach (b) shows a modified version where M_3 allows equalizing the V_{DS} of M_{10} and M_{11}. This allows operation of the circuit even when M_{11} is not in saturation, increasing the input range. An alternative configuration using an input differential pair is shown in (c). These topologies correspond to the followers presented in Figures 3.24 and 3.25 with replicated output branch.

3.9 Design of Highly Linear Tuning Schemes

Continuous tuning is usually required in Gm-C filters to compensate for process RC variations. Theoretically, either the transconductance or the capacitance values can be tuned in order to change the cutoff frequency of the circuit, although tuning of the transconductance value is usually chosen. Typically a tuning range of about 50% is required for this task. An inefficient tuning strategy may lead to a loss of linearity, so the tuning scheme should be carefully selected in order to find the optimal approach that allows minimizing the degradation of linearity and at the same time preserving the performance of the circuit. This section is focused on explaining continuous tuning strategies.

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3.9.1 Adjustment of V-I Conversion Resistors

The first proposal, and the simplest one, is shown below.

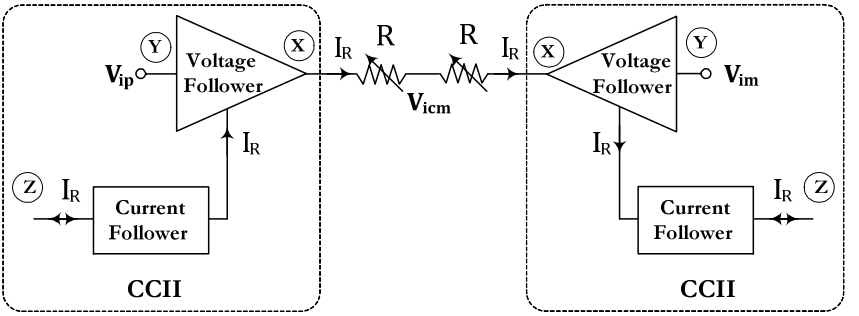

Figure 3.34. Transconductor tuning adjusting the resistor used for V-I conversion

This tuning strategy consists in varying the resistance employed for V-I conversion ([65], [66]), considering that this variation implies a change in the transconductance value.

As passive resistors cannot be used for the conversion if tuning is needed, there is going to be a consequent degradation of linearity and a strong dependence of the performance of the transconductor on tuning. Typically, MOS transistors in triode region are employed to implement those variable resistors and tuning is accomplished by modifying their gate voltage.

Depending on the needs, different configurations of the active resistors can be employed, like parallel or series transistors. Moreover, a choice between PMOS or NMOS transistors has to be made based on the input of the circuit. Finally, as discussed in the previous chapter, QFG components can be added in order to linearize the V-I conversion.

3.9.2 Scaling Output Currents

An alternative approach, shown in Figure 3.35, is based on scaling the output currents, which can be achieved by providing gain or attenuation to the current followers.

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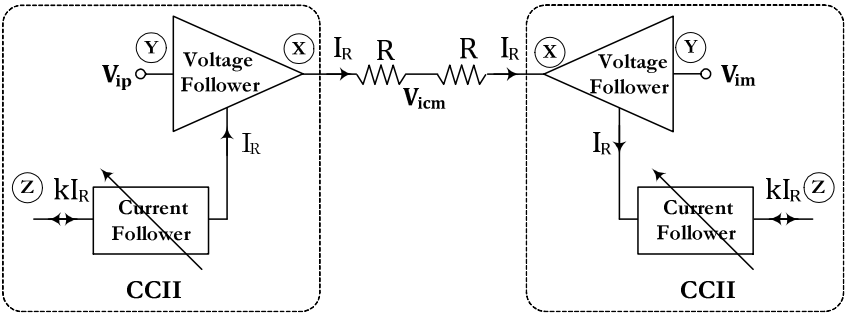

Figure 3.35. Transconductor tuning scaling the output currents

Linearity obtained with this strategy is usually better than in the previous method, as the inner V-I conversion core is not modified and passive resistors can still be used for the conversion. Besides, performance is going to be more stable over the whole tuning range.

Current scaling can be carried out e.g. using transconductance multipliers [26]. Another recent proposal of implementation consists in using programmable differential current mirrors operating in moderate inversion to achieve output current scaling [34], [58].

3.9.3 Array of Transistors and Passive Resistors

The following tuning technique consists in creating an array of passive resistors in series with variable resistors, implemented by MOS transistors in triode region. Some switches are included in order to control the different rows of the array. This approach is illustrated in Figure 3.36.

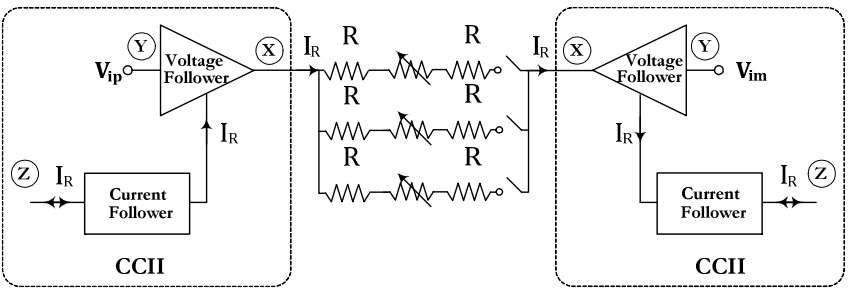

Figure 3.36. Transconductor tuning using an array of transistors and resistors

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Passive resistors are in charge of discrete tuning, while triode transistors carry out continuous one. Lastly, switches, depending on their position, fix which rows of the array are employed to calculate the resistance at a particular moment.

If this strategy is chosen, a tradeoff between linearity and silicon area employed must be reached. The more rows in the array, the more linear the circuit will be, but also more resistors and transistors are needed, thus the more area occupied.

3.9.4 Resistive Current Division

Another possibility, and the one employed in this work, is shown in Figure 3.37.

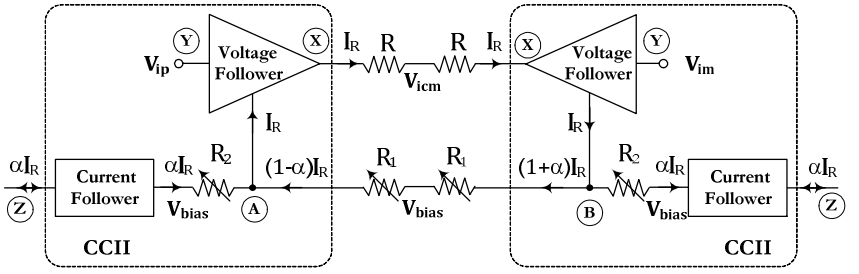

Figure 3.37. Transconductor tuning using resistive current division

According to the figure, a resistive divider splits the output current, thus leading to current attenuation [7], [25], [31] since current followers receive less current, αI_R, than the total amount obtained at the passive resistors, I_R. If resistors are made programmable, attenuation can be adjusted.

The value of α must be calculated to discover the amount of current that goes through the buffers and how much is dismissed. Figure 3.37 shows that the transconductor core provides a differential output current $2I_R$ where $I_R=V_{id}/2R$. Assuming that the input node of the followers is a signal ground with voltage set to V_{bias}, and applying the KCL to nodes A and B, it is obtained that

$$\alpha = \frac{1}{1 + R_2/R_1} \qquad (3.37)$$

Hence the output current is attenuated by a factor α that can be adjusted by the ratio R_2/R_1, and the total transconductance of this circuit is $2\alpha I_R/V_{id}=\alpha/R$. At nodes A and B complementary voltages are generated, given by

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$$V_A = V_{bias} - \alpha R_2 I_R = V_{bias} - \frac{R_1 || R_2}{R} V_{id}$$
$$V_B = V_{bias} + \alpha R_2 I_R = V_{bias} + \frac{R_1 || R_2}{R} V_{id} \qquad (3.38)$$

Therefore assuming matched R_1 resistors, a differential signal ground is generated at the common terminal of R_1 resistors with voltage equal to V_{bias}.

Although this technique is based on adjusting resistance values as in 3.9.1, it has some important advantages. Not only tunable resistors do not modify the V-I conversion core and passive resistors still do the conversion, but also tuning accuracy depends on ratios of resistors, and not on the absolute value of a resistor. This makes tuning more linear and less dependent on thermal and process variations. Besides, since tuning does not rely on the absolute value of the tuning resistors, tuning resistances can be made small so that voltage swing at the terminals of the tuning resistors is minimized. Hence they lead to less distortion as compared to tuning the V-I conversion resistor in the transconductor or in a MOSFET-C filter, which experiences the full input signal swing.

3.9.5 Resistive Current Splitting

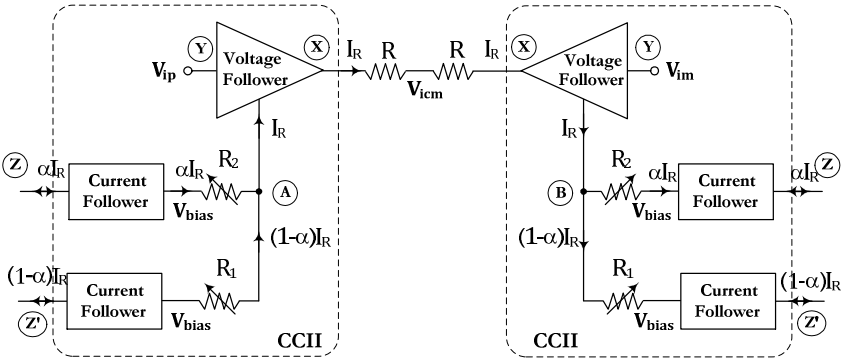

Figure 3.38. Transconductor tuning using resistive current splitting

An alternative approach is proposed and shown in Figure 3.38. Expressions (3.37) and (3.38) remain valid, but it has an advantage with respect to the previously explained tuning scheme, which is that an additional output current $(1-\alpha)I_R$ is also available at the output. Hence the circuit implements two transconductors with high current efficiency sharing a common input, one with transconductance α/R and the other one with transconductance $(1-\alpha)/R$,

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providing increased design flexibility. However, it has also important disadvantages like the additional current followers required, and that mismatch in R_1 resistors now affects linearity.

3.10 Design of Class AB Transconductors

Several techniques have been proposed in section 3.1 to improve linearity of transconductors, but they often require generating extra currents thus increasing the area and power requirements, and/or rely on the MOS square law which is unrealistic in modern processes. A very interesting alternative, also previously proposed, is the use of resistive degeneration by passive resistors for V-I conversion. Unfortunately, as described in section 3.9, it is not a suitable solution when continuous tuning is needed. The use of MOS transistors in triode region instead to implement the resistance element allows continuous tuning but degrades linearity noticeably. Besides, class AB operation is required in the transconductor to allow improving the dynamic performance of the circuit, without increasing its static power consumption. A good way of achieving it is by using QFG and FG techniques, already discussed.

A systematic design approach to achieve micropower class AB CMOS transconductors is presented in this section [64]. Obviously, this new family of high-performance power-efficient transconductors will be based on the use of class AB second-generation current conveyors (CCIIs) [27], already explained in this chapter, as well as on the other circuits proposed in other sections of chapter 3, whose only purpose was helping implementing the most suitable transconductor. The proposed approach includes techniques to get rail-to-rail operation and continuous transconductance tuning, based on FG and QFG transistors.

Regarding the choice of the topology of the circuit and the implementation of the CCII, first steps while designing a transconductor, they must be selected among the proposals of sections 3.3 and 3.8, respectively. In fact, Figure 3.39 shows the complete synthesis procedure that must be followed to obtain a new family of class AB CMOS transconductors.

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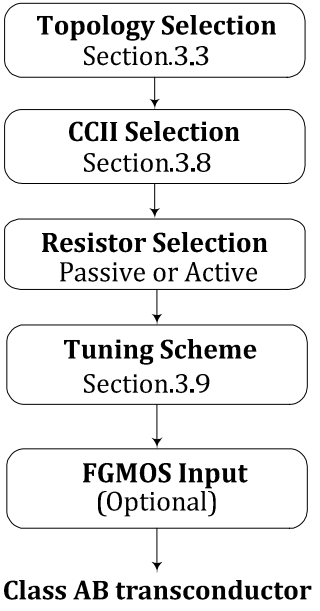

Figure 3.39. Synthesis procedure

The design procedure is as follows:

1) Topology choice based on input resistance or input range requirements. If high input resistance is required, as in G_m-C filters, the topology of Figure 3.8 is chosen. However, if the priority is achieving a rail-to-rail input range but input resistance can be low, another topology should be employed, e.g. Figure 3.10.

2) Choice of the CCIIs of the transconductor based on its requirements. Any circuit of section 3.8 can be selected. Figure 3.32 shows the simplest one, useful when static power must be minimized and a dc level shift between input and output can be tolerated. If the dc level shift must be compensated, circuit of Figure 3.33 (a) is the best option. Topology (b) compensates the shift, but also improves input range; thus it is preferable when input range specification is relevant. FG techniques can also be used to increase the input range if a topology without rail-to-rail input range has been chosen for the transconductor. However, if noise performance must be optimized topology (b) is preferable since it avoids the input attenuation of the FGMOS capacitive divider. Finally, option (c) also compensates the shift and improves linearity, but input range is not increased and

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features less bandwidth than the other CCIIs due to the required internal compensation. So it is preferable when linearity in a limited input range is the key design factor, while speed or input range is not critical.

3) Resistor implementation. When linearity is the key factor and transconductance tuning is not required, the use of passive resistors is preferable. If tuning is needed, then an active implementation must be chosen. A tuning scheme can be selected among the possibilities presented in section 3.9 depending again on the requirements of the transconductor.

Among the options resulting from this procedure (which can be increased by adding extra CCII, active resistor implementations, or different tuning methods), 12 transconductors have been designed, fabricated and measured. The chosen configurations are described in Table 3.3.

Table 3.3. Measurement results of transconductors

Transconductor	**1**	**2**	**3**	**4**	**5**	**6**
Topology	3.8	3.8	3.8	3.8	3.8	3.8
CCII	3.32	3.32	3.33(a)	3.33(a)	3.33(b)	3.33(b)
Active resistor	No	Yes	No	Yes	No	Yes
FGMOS input	No	Yes	No	No	No	No
Technology	0.5u	0.5u	0.5u	0.5u	0.5u	0.5u
Supply vol. (V)	3.3	5	3.3	3.3	3.3	3.3
THD @100kHz @2V	-46dB	-58 dB	-50dB	-30dB	-35dB	-31dB
Noise (nV/√Hz)	39	98	40	40	43	43
Power (mW)	0.23	2.20	0.30	0.30	0.33	0.33
Silicon area (mm^2)	0.06	0.07	0.06	0.07	0.06	0.07
Transconductor	**7**	**8**	**9**	**10**	**11**	**12**
Topology	3.8	3.10	3.10	3.10	3.10	3.10
CCII	3.33(c)	3.33(a)	3.33(a)	3.33(b)	3.33(b)	3.33(c)
Active resistor	No	No	Yes	No	Yes	No
FGMOS input	No	No	No	No	No	No
Technology	0.5u	0.5u	0.5u	0.5u	0.5u	0.5u
Supply vol. (V)	3.3	3.3	3.3	3.3	3.3	3.3
THD @100kHz @2V	-32dB	-56dB	-43dB	-48dB	-51dB	-49dB
Noise (nV/√Hz)	31	40	42	44	43	32
Power (mW)	0.26	0.30	0.30	0.33	0.33	0.26
Silicon area (mm^2)	0.07	0.06	0.07	0.06	0.07	0.07

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Concerning second-order effects and noise analysis, the discussion of section 3.5.2.3 remains valid. In that section, those parameters have been explained related to the class AB SSF so, as these new systematically obtained transconductors have been based on that circuit, their features are similar. However, note that each developed transconductor would have its own noise expression derived from the original one, depending on its structure.

The chip containing the 12 transconductors was fabricated in a 0.5µm double-poly n-well CMOS technology with nominal NMOS and PMOS threshold voltages of 0.67 V and –0.96 V, respectively. A microphotograph is shown in Figure 3.40. Table 3.3 summarizes the measurement conditions and the main results obtained. Linearity is evaluated for large signal levels, which generate signal currents much larger than the quiescent currents. Despite this fact, that would avoid operation of a conventional class A transconductor, linearity is still reasonably good for the class AB transconductors. This way, linearity can be obtained for large input signals in transconductors featuring micropower quiescent consumption. Among the transconductors, the ones presenting topology 3.10 have in general better linearity since V-I conversion takes place at the input terminal, but the driving stage is resistively loaded. Obviously, linearity is better when passive resistors are employed, but then tuning is not available. Transconductor 2 has better linearity than the rest since a higher supply voltage was employed and because the FGMOS input stage attenuates the input signal. However, input-referred noise level is increased due to the input attenuation.

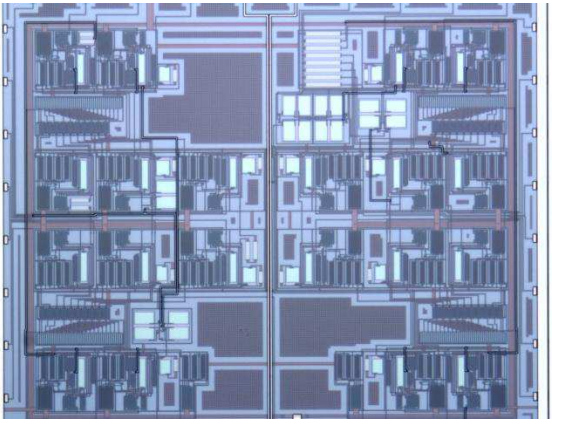

Figure 3.40. Chip microphotograph

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Some measurements have been done to illustrate the operation of the circuits. Figure 3.41 shows the measured IM3 of transconductor 1 for two input tones of 1Vpp each (total input 2Vpp) and frequencies of 950 kHz and 1050 kHz. The resulting IM3 is -56dB. Figure 3.42 shows the harmonic distortion measured for a differential input sinusoid of 100 kHz and different amplitudes. The bias current was I_B=50 μA. As expected, harmonic distortion is dominated by the third-order harmonic. For peak-to-peak differential input voltages larger than $4RI_B$=2•50μA•3.75kΩ=0.7 V the output currents are larger than the bias current I_B. Note that beyond this point in Figure 3.42 linearity is not degraded abruptly, confirming the class AB operation of the circuit. For instance, Total Harmonic Distortion (THD) is lower than -55 dB for an input of 1.2 Vpp (36 % of the supply voltage), which corresponds to output currents 60 % larger than I_B. If for this input I_B is reduced to 10 μA, measurements show a THD still low (-49 dB), and in this case the output current is 800% times larger than I_B. Figure 3.43 shows the amplitude spectrum of the output for an input of 1 Vpp and 1 MHz, showing a THD = -59.47dB.

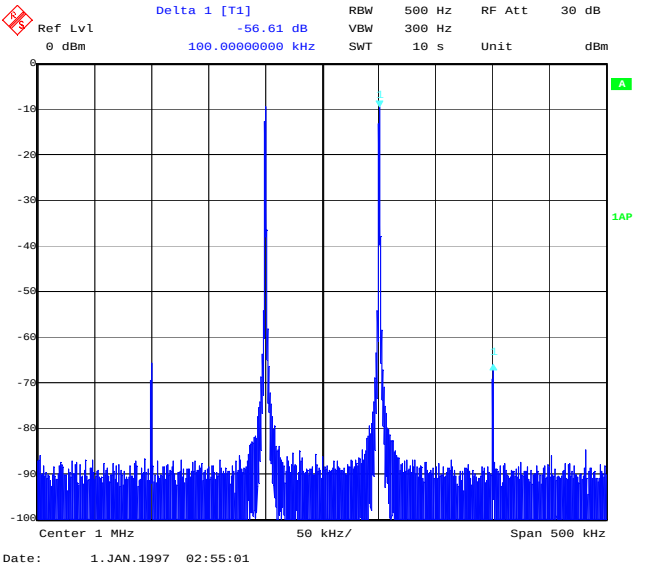

Figure 3.41. IM3 of transconductor 1 for two input tones of 1Vpp

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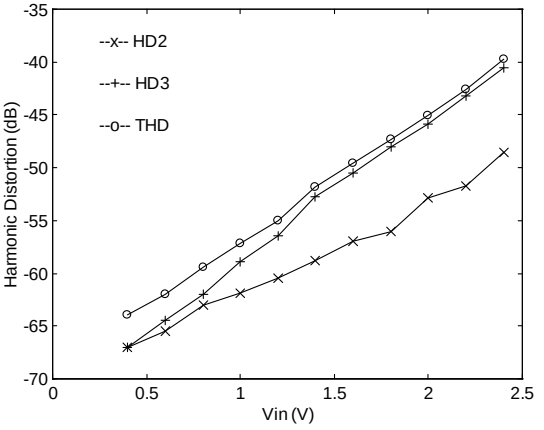

Figure 3.42. Measured harmonic distortion vs input voltage at 100kHz

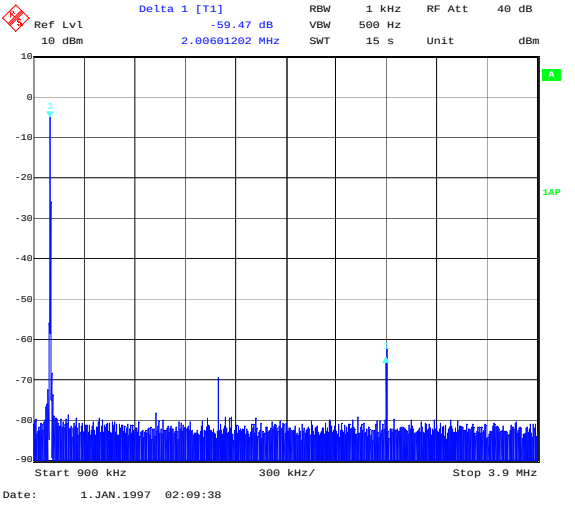

Figure 3.43. Measured output amplitude spectrum for an input tone at 1MHz

Moreover, Figure 3.44 shows the measured transfer characteristics of transconductor 2 obtained using a low-frequency periodic input ramp. Note the rail-to-rail input range and the ability to change transconductance value by the tuning voltage of the active resistor. Figure 3.45 shows the measured output spectrum of transconductor 2 for two input tones of 950 kHz and 1050 kHz and 0.5Vpp (total input 1Vpp) resulting in an IM3 of -74.66 dB. When the amplitude of each input tone increases to 2Vpp, IM3 is -52.13 dB.

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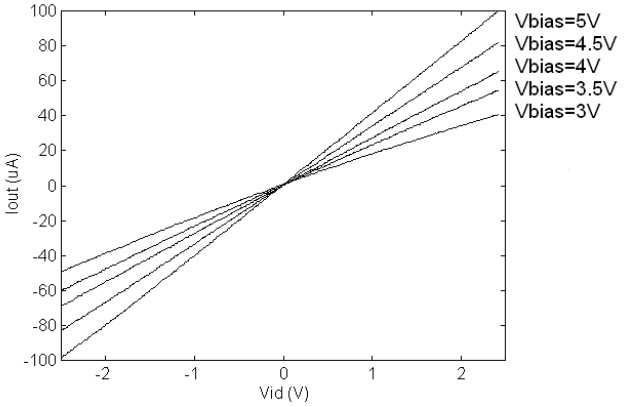

Figure 3.44. Transfer characteristics of transc. 2, tuning voltage ranging from 3V to 5V

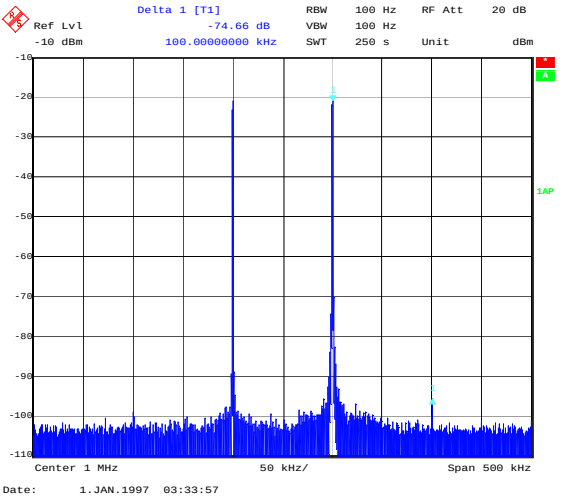

Figure 3.45. Output amplitude spectrum for two input tones at 950 kHz and 1050 kHz

According to the measurements, the proposed transconductors have a good trade-off between linearity and power consumption, with a reasonable area despite the extra capacitors required by the FGMOS and QFGMOS transistors.

3.11 Summary

Design of high-performance CMOS transconductors, widely used in several applications [10], is challenging nowadays due to the limited signal swing

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available under the reduced supply voltages imposed by technology downscaling and low power requirements. Usually the applications demand the availability of transconductors featuring high linearity in a wide input range under the aforementioned low supply voltage requirements.

This chapter has been focused on designing suitable transconductors for wireless receivers, by using a systematic approach. According to already mentioned current demands, the new generated family of transconductors feature class AB operation as well as continuous tuning of its transconductance value.

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CHAPTER 4

Highly-linear tunable Gm-C filters design for channel selection

Channel select filters are required in wireless receivers to discriminate the signal in the desired channel from other undesired signals in adjacent channels, interferences, and out-of-band noise. They are usually continuous-time band-pass filters if the Intermediate Frequency (IF) of the receiver is not zero, or continuous-time low-pass filters in direct conversion receivers (having zero IF). The current trend in wireless receivers is toward solutions featuring high integration density and low power consumption. To achieve these requirements low-IF and zero-IF receiver architectures with active filter implementations are used. However, large interferers near the desired signal demand high linearity, which is often difficult to achieve together with low area and low power consumption. Although active-RC filters are widely employed due to their high linearity, also transconductance-C (G_m-C) topologies have been proposed (e.g.[1–4]). As discussed in the previous chapter, due to their open-loop operation, G_m-C filters usually achieve lower power consumption for a given bandwidth, but they also feature less linearity. In order to solve this limitation, the basic trend is designing the transconductors by coming back to the classic approach to achieve highly linear circuits, by the use of negative feedback and passive resistors, providing a highly linear voltage-to-current (V-I) conversion. This way, linearity levels comparable to those of active-RC filters have been reported [5].

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Channel selection filters are customarily designed to allow the required dynamic range in the worst-case scenario, that is, in the presence of the largest interferers expected. Since these interferers appear very rarely, the filter operates with excessive dynamic range most of the time. This has a strong penalty on power consumption, which increases proportionally to the dynamic range. To avoid this drawback various approaches have been suggested based on adaptive biasing of the filter [6–9]. However, a typical shortcoming is that adaptation of the dynamic range is not instantaneous, limiting the ability to handle large blocker signals. A relatively fast and efficient dynamic range adaptation technique was proposed in [10]. Here we employ an alternative approach based on class AB operation of the filter. This way an inherent instantaneous adaptive biasing is achieved which preserves high linearity for large inputs using low quiescent currents. To illustrate this approach we present a low-pass G_m-C filter suitable to the demands in terms of linearity and power consumption of channel selection filters in highly integrated zero-IF receivers for various wireless standards. In particular, it could be applied as a dual-mode filter intended to meet specifications for the Bluetooth [11] and 802.15.4 [12] standards. These receivers would enable to add very simple 802.15.4-based connectivity (e.g. using ZigBee) to mobile phones, where Bluetooth is already incorporated. This would expand the applications of the mobile phone, including lighting and access control, patient/fitness monitoring, etc. [2].

Transconductors employed in the filters, based on chapter 3, achieve high linearity by the use of a passive resistor for V-I conversion and the use of negative feedback in the voltage followers that translate the input voltage to the resistor terminals. Moreover, their transconductance tunability allows adaptation of the filter cutoff frequency to multiple standards and compensation for process variations. Note that, in order to improve the G_m-C filter, tuning cannot be done manually, but with an automatic tuning system. Besides, transconductors (and hence filters as mentioned above) operate in class AB, allowing low quiescent power consumption without degradation of dynamic performance. The filter has been designed and implemented in a 0.5µm CMOS technology, and measurement results are presented.

This Chapter is organized as follows. Section I describes the direct conversion receiver architecture which employs the channel selection filter proposed. The first approach to the design of channel selection filters for Bluetooth is covered in Section II, achieving at the end of it a novel circuit. In Section III some modifications to the previous design are made, in order to

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improve it and adapt it better to current requirements. Finally, conclusions are drawn in Section IV.

4.1 Direct Conversion Receivers

Among the architectures for receivers, super-heterodyne receiver is one of the most employed as it allows obtaining high sensitivity and frequency selectivity, despite its problems to be integrated on silicon. It is typically a dual conversion architecture, in which, at the first stage the RF signal is down-converted to IF (intermediate frequency) and then, in the second stage it is down-shifted from IF to baseband signal. The block diagram of a typical super-heterodyne receiver is shown in Figure 4.1.

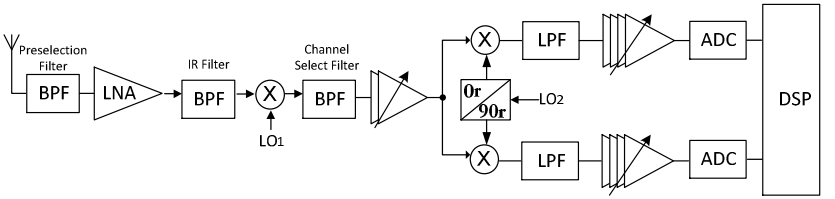

Figure 4.1. Super-heterodyne receiver

One major disadvantage to the super-heterodyne receiver is the problem of image frequency, which is the undesired frequency band equidistant regarding the frequency of the first local oscillator to the desired RF signal band. If there is interference at the image frequency band, it is also going to appear next to the useful signal after the intermediate frequency mixer. Hence it cannot be eliminated by filtering at the IF section. For that reason, the receiver requires an image-reject filter to attenuate the signals at image band frequencies just before the conversion to IF. If a high IF is chosen, image frequency would be very far from the desired signal and a simple filtering would be required. However, the intermediate frequency filter must have very high selectivity in order to properly select the desired channel and attenuate the adjacent ones.

The first mixer usually has a variable frequency oscillator as an input, in charge of selecting the desired channel. This allows establishing a constant intermediate frequency, independent of the channel to demodulate and, therefore, a fix IF filtering, simplifying its design. The channel selection is normally achieved through the IF filter, critical in determining the sensitivity and selectivity of a receiver.

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The superheterodyne architecture allows distribution of gain, noise figure and filtering across different frequency ranges, providing good noise and interference performance. Besides, its design is easier than others. However, it also requires many external components, including the RF, image and IF band-pass filters, making it bulky and expensive. Moreover, low consumption is difficult to achieve with these receivers. As a possible solution to the high consumption and the low integration level, Low-IF heterodyne receivers have been proposed. Although they are not able to completely overcome these issues, they may significantly reduce them. In these receivers image frequencies are usually eliminated in baseband by digital signal processing of phase and quadrature components. Due to this, RF filters can be less selective but, as an inconvenient, image-rejection is degraded when the branches that process phase and quadrature components are not identical. Nowadays, it is the most employed architecture for Bluetooth or Zigbee receivers, with typical intermediate frequencies ranging from 1 to 2 MHz.

As it has been already said, current trends are focused on implementing circuits featuring high integrating levels and low power consumption. Consequently, direct conversion receivers are becoming more and more popular. They are also known as Zero-IF receivers, as they do not have any intermediate frequency. Figure 4.2 illustrates this architecture.

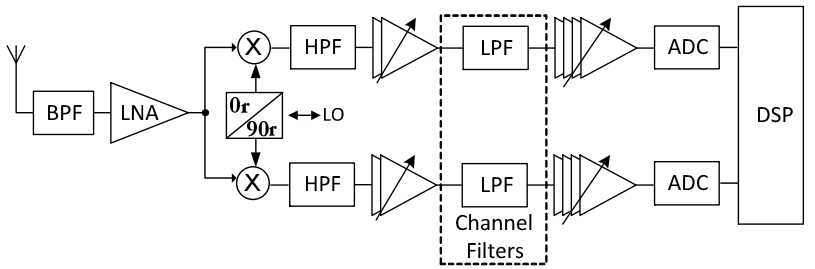

Figure 4.2. Homodyne receiver or Zero-IF

In this scheme, the desired signal is directly translated to baseband, where a simple low-pass filter can be employed to select the channel that is going to be demodulated. This filter is also useful to avoid aliasing in the subsequent A/D conversion if there is a digital demodulation. Being at low-frequency, the filter has lower consumption and it does not need a high selectivity (high orders are not needed), making its integration easier. Besides, by using this topology, the image frequency issue is overcome, so external components are not necessary.

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For all these reasons, direct conversion receivers present a good tradeoff regarding cost, size, and power consumption.

Nevertheless, they have also important shortcomings. Firstly, their DC-offset, which cannot be eliminated since the signal has been translated to baseband, and can corrupt it or saturate the baseband section stages with a high input voltage. This DC offset may be generated by self-mixing at the mixer previous to the baseband section, due to the finite isolation between the mixer inputs. And secondly, the flicker Noise (1/f noise) that appears at low frequencies. It can be avoided by setting high gain at the RF section because the requirements of Noise Figure at the baseband section are reduced, but this also increases the linearity requirements. To avoid saturation of the baseband stage due to the offset and to attenuate flicker noise, a first-order RC high-pass filter is often employed after the mixer. The cutoff frequency of this filter represents a tradeoff between rejection of flicker noise and degradation of the low-frequency content of the received signal (whose impact is strongly dependent on the modulation employed). Typical values are around a few tens of Hz [13]. The cutoff frequency of the channel selection filters also depends on the modulation employed, and a wide frequency tuning range is required to allow multiple standards.

Due to their mentioned advantages, direct conversion receivers have been chosen for this work. Therefore, their different blocks, like channel selection filters, are going to be implemented based on their requirements.

4.2 Design of Channel Selection Filters for Bluetooth (1)

When the Zero-IF receiver presented in Figure 4.2 is employed for Bluetooth or Zigbee standards, the system-level specifications set the particular specifications for the analog low-pass channel-select filter included in the diagram, as it is shown in Table 4.1.

The order required for the filter is determined by the amount of channel-selection filtering performed in the analog and digital domains. In our receiver system-level simulations show a good performance tradeoff by using a third-order Butterworth analog filtering. This type of filter represents the best tradeoff between reduced in-band ripple and small group delay distortion [14]. Also component values are usually less critical than in other filters [15]. Concerning linearity and noise specifications, they can be traded off by adjusting the pre-filter and post-filter amplifier gain.

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Table 4.1. Specifications for analog LPF in Zero-IF Receiver for Bluetooth and Zigbee

Parameter	Bluetooth/Zigbee
Power	5 mW
Filter order	3
Cutoff frequency	650 kHz / 1.2 MHz
IIP3	> +18dBVp
Output noise spectral density	225nV/√Hz

4.2.1 Transfer Function

The schematic of the low-pass filter designed is shown in Figure 4.3. It employs six tunable transconductors and six matched grounded capacitors. The first two transconductors along with the first pair of grounded capacitors form a first-order filter, and the subsequent four transconductors plus the other four capacitors form a Tow-Thomas second order section. A unity-gain buffer is used at the output stage to avoid loading of the filter output by the capacitance of the bonding pads. Load resistance connected to the buffer, R_L, must have the same value as the filter resistance in order to achieve input and output voltages approximately equal.

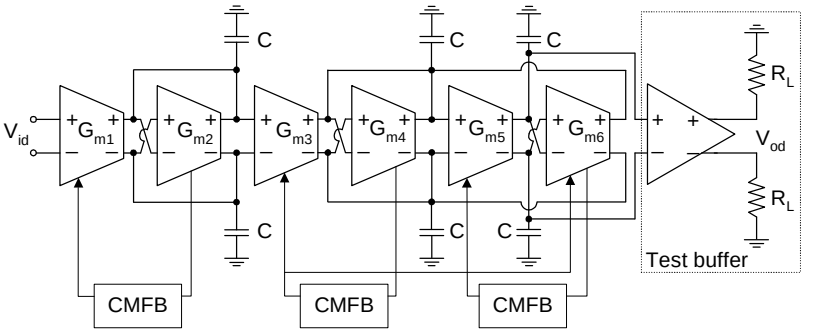

Figure 4.3. Third-order Butterworth G_m-C channel filter

As it is a fully differential implementation, common-mode control circuitry is needed at some nodes. The CMFB circuit employed is shown in Figure 4.4. The output common-mode voltage V_{ocm} of a transconductor is obtained by sensing the input common-mode voltage V_{icm} of the transconductor it drives. This voltage is down-shifted by M_{10} to compensate for the DC up-shift of transconductor's input transistor, M_1.

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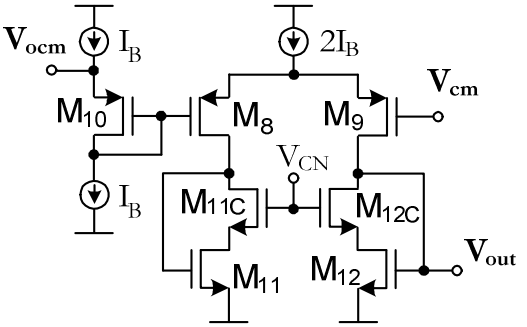

Figure 4.4. CMFB circuit

The transfer function of the filter is

$$H(s) = \frac{V_{od}(s)}{V_{id}(s)} = \left(\frac{G_{m1}/C}{s + G_{m2}/C}\right) \cdot \left(\frac{G_{m3}G_{m4}/C^2}{s^2 + s\,G_{m4}/C + G_{m5}G_{m6}/C^2}\right) \quad (4.1)$$

Regarding transconductances, it is convenient to set $G_{m1} = G_{m2} = G_{m4}$ and $G_{m3} = G_{m5} = G_{m6}$.

4.2.2 Design of the Transconductor

This Section is focused on describing the design of the transconductor finally employed in the Gm-C channel selection filter, along with a detailed performance analysis [16].

4.2.2.1 Transconductor Diagram

The diagram of the transconductor employed is shown in Figure 4.5. A preliminary version of the transconductor design supported by simulations was presented in [17]. Voltage-to-current conversion is based on two second-generation current conveyors (CCIIs 1 and 2) and passive resistors R. In the proposed transconductor the differential input voltage is replicated at the terminals of resistor 2R, achieving a highly linear V-I conversion. The resulting resistor current $I_R=V_{id}/(2R)$ is conveyed to the high-impedance Z output. Resistor 2R is split in two matched resistors R to extract the input common-mode voltage V_{icm}, which is used to sense the output common-mode voltage of the driving stage [18].

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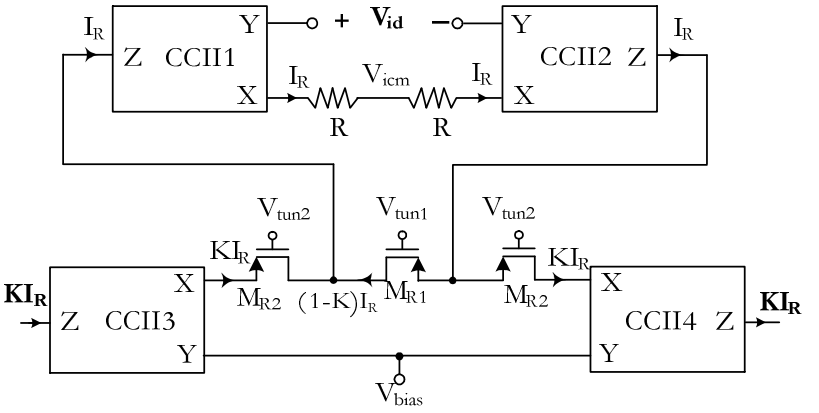

Figure 4.5. Transconductor Diagram

In order to provide transconductance tuning, a resistive divider implemented by transistors in triode region is used at the output of the V-I conversion stage [5], [19], [20]. The divider splits current I_R in two branches, yielding a differential output current $2KI_R$ where $K=1/(1+2R_2/R_1)$ and R_2 and R_1 are the channel resistances of transistors M_{R2} and M_{R1}, respectively. Thus the total transconductance is $G_m=2KI_R/V_{id}=K/R$ and can be tuned by DC voltages V_{tun1} and V_{tun2}. Assuming a first-order model for the transistor in triode region, expression for the current attenuation K becomes

$$K = \frac{1}{1+\frac{2R_2}{R_1}} = \frac{1}{1+2\frac{(W/L)_1}{(W/L)_2}\frac{(V_{tun1}-V_{S1}-V_{TH})}{(V_{tun2}-V_{S2}-V_{TH})}} \qquad (4.2)$$

According to the figure, CCIIs 3 and 4 act as current followers, creating a signal ground at the output of the resistive divider set to a DC voltage V_{bias} and conveying the resistive divider current to the high-impedance output terminal.

As it has been said in previous chapters, the use of active resistors for transconductance tuning has less impact on performance than the use of these devices for V-I conversion in source-degeneration transconductors for various reasons [5]. First, the tunable resistors do not modify the V-I conversion core. Second, tuning accuracy depends on ratios of resistors, and not on their absolute value. This makes tuning more linear and less dependent on thermal and process variations, and allows freedom on the choice of the absolute resistance values. Hence they can be small so that voltage swing at the terminals of the tuning resistors is minimized, leading to less distortion as compared to tuning the V-I

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conversion resistor in the transconductor or in a MOSFET-C filter, which experiences the full input signal swing.

4.2.2.2 Class AB CCII

In order to achieve class AB operation for the transconductor of Figure 4.5, its CCIIs must operate in class AB. The proposed implementation for the class AB CCIIs, described in Chapter 3, is shown in Figure 4.6.

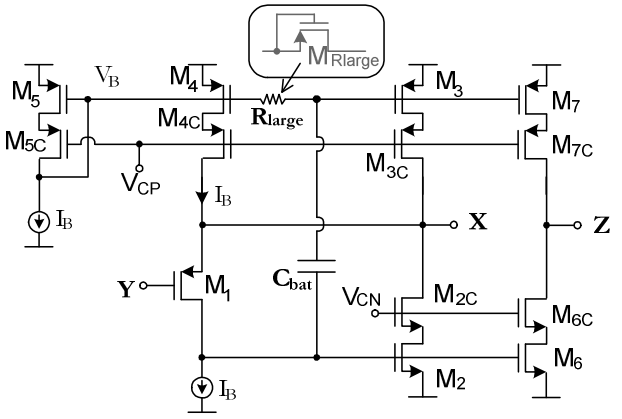

Figure 4.6. Class AB CCII employed

A voltage follower replicates voltage from terminal Y to terminal X. It is made by the source follower transistor M_1 and transistors M_2-M_{2C} which provide negative feedback. Transistor M_1 carries a constant current I_B, which neglecting second-order effects leads to a constant source-to-gate voltage V_{SG1}. This feature improves linearity as compared to the conventional source follower. Transistor M_3 is a QFG transistor [21] and provides class AB operation. It has a stable DC bias voltage set through a large valued resistive device R_{large}, and a signal voltage coupled by a floating capacitor C_{bat}.

Note that while R_{large} and C_{bat} do not modify static performance and quiescent current of M_3 is accurately controlled by the current mirror M_3-M_5, is supply, process, and temperature independent, and can be made small to save static power, they do improve dynamic performance. The fact that the gate voltage of M_3 becomes signal-dependent, provides extra output transconductance and allows class AB operation. The dynamic performance of this circuit has been already explained in detail in Section 3.8.

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It has also been mentioned before that a RC high-pass filtering occurs between the gates of M_2 and M_3. Resistance Rlarge should be high enough to provide a cutoff frequency lower than the minimum frequency component of the input signal. In baseband applications usually only the DC component should be blocked, requiring a very large resistance of GigaOhms. Needless to say that, by implementing it by the leakage resistance of a minimum-size diode-connected MOS transistor in cutoff region, the purpose is accomplished. Note that in our application the lowest signal frequency to be processed is around 50 Hz thanks to the high-pass filter after the mixer. This relaxes even more the minimum required value for R_{large}.

4.2.2.3 Small-Signal Analysis and Stability

The proposed transconductor uses negative feedback loops to improve accuracy, so proper design is required to enforce stability. Note from Figure 4.6 that a two-pole negative feedback loop is used. The dominant pole corresponds to the high-impedance internal node (gate of M_2) and the non-dominant pole is set by node X. Considering that the circuit of Figure 4.6 is totally based on the class AB SSF, studied in Chapter 3, the small-signal analysis developed in Section 3.5.2.1 is still valid, and the different expressions do not need to be repeated here.

It must be remembered that the conclusion, after all the calculus, was that in order to enforce stability, f_{nd} should be at least twice the gain-bandwidth product of the loop, i.e., $f_{nd} > 2|A_{ol}|f_d$, and that led to

$$C_X < \frac{1}{2}\frac{g_{m1}+g_{mb1}}{(g_{m2}+\alpha g_{m3})\left(1+\frac{r_B}{r_{o1}}\right)}C_{G2} \qquad (4.3)$$

Note that for low load capacitances at terminal X, proper transistor aspect ratios allow enforcing stability. This is the case in the CCIIs of the transconductor of Figure 4.5, where terminal X is resistively loaded. Otherwise, if condition (4.3) is not met, then a compensation capacitor connected to the gate of M_2 can be used to increase the capacitance at this node. Note also that if M_1 is embodied in an individual well connected to the source terminal (as done in this work), then g_{mb1} does not appear in the above expressions, and the well-to-substrate capacitance of M_1 increases C_X. Therefore the maximum allowed value for C_X in (4.3) is reduced in this case.

The approximate closed-loop bandwidth of the Y-X voltage transfer, being f_{nd} higher enough than f_d, is going to be repeated as well

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$$f_{-3dB} \approx |A_{ol}|f_d \approx \frac{g_{m2} + \alpha g_{m3}}{2\pi C_{G2}}\left[1 + \frac{r_B}{(g_{m1} + g_{mb1})r_{o1}r_{o2}}\right] \qquad (4.4)$$

Note that the extra output transconductance provided by the QFG technique and corresponding to the term αgm3 in the expressions above, increases closed-loop bandwidth.

4.2.2.4 Second-Order Effects and Noise Analysis

Second-order effects and noise analysis are also similar to the class AB SSF ones, explained in Section 3.5.2.3. Geometric and parametric mismatch, as well as temperature and supply voltage variations may occur in practice and they should be considered in the design. As mentioned above, the transconductor features well controlled quiescent currents regardless of supply or temperature variations. This is because quiescent currents are set by current mirroring, so provided that bias current I_B is independent of these variations quiescent currents are independent too. The V-I conversion core is also highly insensitive to mismatch since it relies on negative feedback loops and passive resistors. Variations in the parameters or the dimensions of the transistors in the input followers are not relevant as long as the loop gain is kept high enough. However, mismatch in the transistors implementing the current mirrors alters the current copy between X and Z terminals and modifies the quiescent currents, so proper layout techniques are required to minimize such mismatch. Note however that the inclusion of class AB operation by the QFG technique does not increase sensitivity to mismatch, process, or temperature variations. Variations in the value of R_{large} or C_{bat} due to process or temperature changes do not affect static performance, they just modify the cutoff frequency of the high-pass filter created by their inclusion, which is irrelevant as long as the resulting frequency remains below the minimum frequency component of the signal.

Concerning the bulk effect, it may affect transistor M_1 if it is not embodied in an individual well connected to the source terminal. The influence in the small-signal performance is reflected in the g_{mb1} term. In large-signal operation it makes the DC level shift between Y and X terminals dependent on the input signal, degrading linearity. These problems are overcome as mentioned by using an individual n-well for M_1, but in this case the additional source-to-substrate nonlinear capacitance increases parasitic capacitance at the output node and distortion, and should be considered when compensation is designed, as mentioned previously. This effect can also affect cascode transistors, but its

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influence in this case is minor. The rest of transistors have the source tied to the corresponding supply rail, thus not suffering from this effect.

Concerning noise, as it has been highlighted in previous chapters, the main sources in CMOS analog circuits are thermal and flicker noise. Considering thermal noise, the approximate expression for the equivalent input noise density of the transconductor is

$$\overline{v_{N,in}^2(f)} \approx \frac{16}{3} k_B T R^2 \left\{ \begin{array}{l} \left(1+\frac{1}{K}\right)^2 \left[\begin{array}{l} \frac{1}{g_{m1}R^2} + \sum_{i=2}^{7} g_{mi} + \\ +g_{mB}\left(1+\frac{1}{g_{m1}R}\right)^2 \end{array} \right] + \\ +\frac{3}{2}\left(\frac{1}{R}+\frac{1}{R_1}\right) + \frac{3}{K^2 R_2} \end{array} \right\} \qquad (4.5)$$

where k_B is the Boltzmann's constant and T the absolute temperature. Parameter g_{mi} is the transconductance of transistor M_i, g_{mB} is the transconductance of current source I_B, and K is the attenuation in (4.2).

Regarding flicker noise the equivalent input noise density becomes

$$\overline{v_{N,in}^2(f)} \approx \frac{2R^2}{C_{ox}f} \left\{ \begin{array}{l} \left(1+\frac{1}{K}\right)^2 \left[\begin{array}{l} \frac{K_1}{W_1 L_1 R^2} + \sum_{i=2}^{7} \frac{g_{mi}^2 K_i}{W_i L_i} + \\ +g_{mB}^2\left(1+\frac{1}{g_{m1}R}\right)^2 \frac{K_B}{W_B L_B} \end{array} \right] + \\ +\frac{g_{mR1}^2 K_{R1}}{W_{R1} L_{R1}} + \frac{1}{K^2}\frac{g_{mR2}^2 K_{R2}}{W_{R2} L_{R2}} \end{array} \right\} \qquad (4.6)$$

where the constant K_i is dependent on transistor M_i and can vary widely for different devices in the same process. C_{ox} is the gate oxide capacitance per unit area, W_i and L_i the width and length, respectively, of transistor M_i. From (4.5) and (4.6) it can be noticed that the input-referred noise is decreased by increasing the transconductance K/R, and that as K decreases the contribution of the noise in the output CCIIs dominates since their noise is not attenuated. For $R<<1/g_{m1}$, noise of the input transistor M_1 and the current source I_B at the drain of M_1 dominate. The class A version of the transconductor (without M_{Rlarge} and C_{bat}) has the same noise expressions. Hence the use of the QFG technique does not degrade noise performance. This is often not the case in other techniques to achieve class AB operation which require additional circuitry that may increase noise level.

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4.2.2.5 Design Considerations

The transconductance values required in the channel filter will be imposed by the target cutoff frequency and the size of the filter capacitors (selected based on a tradeoff including noise and area requirements). This imposes the required value for R and the range of values for K in (4.2). Transistor dimensions are selected considering the stability condition in (4.3) and the required bandwidth in (4.4). Stability is readily achievable since C_X in (4.3) for the transconductor is relatively low (it is dominated by the poly-substrate capacitance of the high-resistance poly resistor R, of 160 fF according to post-layout extraction). The choice for the dimensions of M_1 is particularly important since it notably influences stability (4.3), linearity and noise (particularly when low R, i.e., large transconductance values, are chosen, as (4.5) and (4.6) reflect). A large W/L value for M_1 is advantageous, increasing g_{m1}, while the L value chosen represents a tradeoff between the input capacitance of the transconductor and the flicker noise. Transistor M_{Rlarge} is implemented with minimum size to reduce area, as mentioned in Section 4.2.2.2. Capacitor C_{bat} can be chosen from 2 to 5 times C_{G3}, to prevent low α values in the high-pass filter expression without representing much area overhead.

4.2.2.6 Measurement Results

The class AB transconductor has been designed and fabricated in a standard 0.5µm CMOS n-well process with nominal nMOS and pMOS threshold voltages of 0.64 V and –0.92 V respectively. For the implementation three metal layers, poly-poly capacitors, and high resistance polysilicon resistors were used.

Table 4.2. Transistor Aspect Ratios

Transistor	Value (µm/ µm)
M_1, M_3, M_4, M_5, M_7, M_{10}	100/1
M_2, M_6	60/1
M_{2C}, M_{6C}	60/0.6
M_{3C}, M_{4C}, M_{5C}, M_{7C}	200/0.6
M_{Rlarge}	1.5/0.6
M_{R1}	400/1
M_{R2}	200/1
M_8, M_9	30/1
M_{11}, M_{12}	15/1
M_{11C}, M_{12C}	100/0.6

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Transistor aspect ratios employed are shown in Table 4.2. Capacitor C_{bat} was implemented with two polysilicon layers and has a nominal value of 1pF while resistor R was implemented with high-resistance polysilicon and has a value of 10kΩ. Measurements were made for a supply voltage of ±1.65 V and a bias current of 10μA. Figure 4.7 shows the measured IIP3 for two input tones of 1MHz and 1.05MHz. A value of 21dBVp is achieved, slightly lower than in simulation (24.5dBVp).

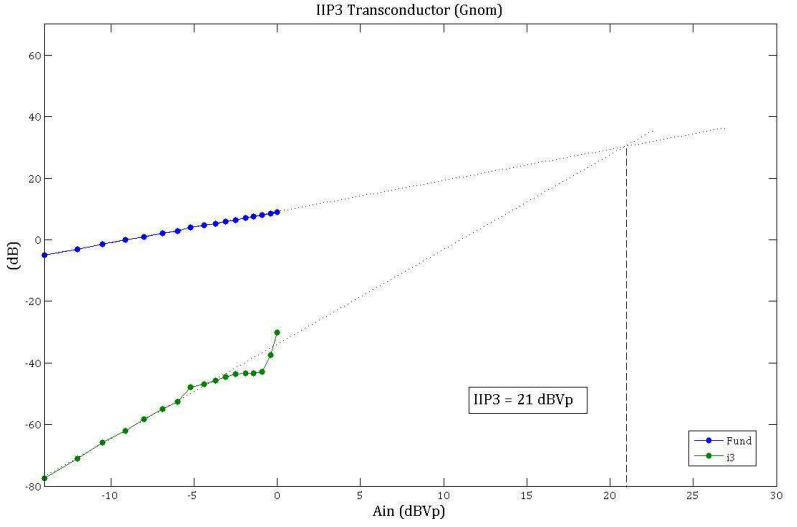

Figure 4.7. IIP3 measurement of the transconductor

Table 4.3 shows the main measurement results obtained. The analytical expression in (4.5) predicts an equivalent input thermal noise density of 142nV/√Hz using the transistor parameters provided by the foundry. It is in reasonable agreement with the noise density measured at 1MHz (107nV/√Hz), which is mainly due to thermal noise, validating the theoretical analysis. Deviations are attributed to the simple analytical model used to calculate g_m and process variations. Input noise measured at 100kHz is 292nV/√Hz, which is dominated by flicker noise. Subtracting the thermal noise, a measured flicker noise of 271nV/√Hz is obtained. The analytical expression in (4.6) yields a value of approximately 320nV/√Hz for the flicker noise at 100kHz.

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Table 4.3. Measurement Results of the Transconductor

Parameter	Value
Technology	0.5μm CMOS
Supply Voltage	±1.65 V
Bias Current	10 μA
IIP3 (In-band)	21 dBVp
IM3@ -8dBVp	59.2 dB
CMRR@ 0.2MHz	56 dB
Eq. input noise density @ 100 kHz	292nV/√Hz
Eq. input noise density @ 1 MHz	107nV/√Hz
Die area	0.25 mm²
Quiescent power	560 μW

4.2.3 Implementation of the Filter and Experimental Results

Once the transconductor is designed, the filter of Figure 4.3 can be finally implemented, as it is its main component. Besides the transconductors, the filter just requires capacitors, a unity-gain buffer, and the CMFB circuits shown in Figure 4.4.

The proposed G_m-C filter was fabricated in the same technology as the transconductor. The microphotograph of the circuit can be seen in Figure 4.8, where the six transconductors, the capacitors and the test buffer can be observed. The six poly-poly filter capacitors were interdigitized to improve matching. The silicon area employed by the filter is 2.22 mm². The supply voltages employed for all the measurements were V_{DD} = 1.65 V and V_{SS} = -1.65 V. The dimensions of the transistors employed in the six tunable transconductors and three CMFB circuits of the filter are listed in Table 4.2. The value of the grounded capacitors of the filter is 15 pF.

In Figure 4.9 the harmonic distortion measured for a differential input sinusoid of 120 kHz and different amplitudes is shown. The filter is set to a nominal cutoff frequency of 1 MHz. The bias current was I_B = 10 μA. Note that harmonic distortion is dominated by the third-order term, as expected from a fully differential filter. For peak-to-peak differential input voltages larger than $4RI_B$=4•10μA•10kΩ = 0.4 V the output currents are larger than the bias current I_B. Beyond this point in Figure 4.9 linearity is not degraded abruptly, confirming

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the class AB operation of the circuit. As can be seen, Total Harmonic Distortion (THD) is lower than -55 dB for an input of 1.2 Vpp (36% of the supply voltage), which corresponds to peak currents 300% larger than the bias current.

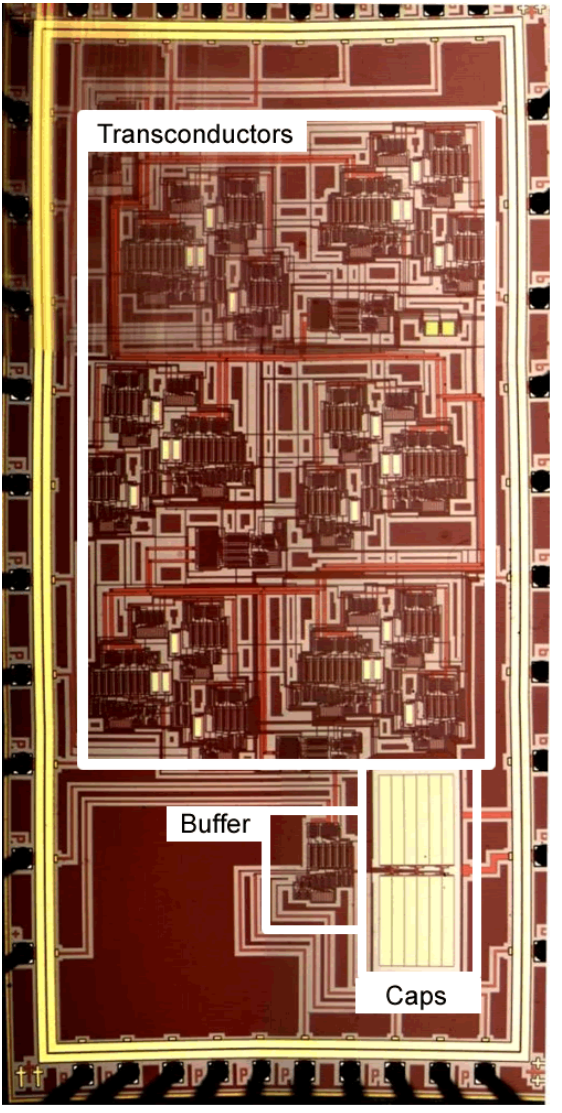

Figure 4.8. Microphotograph of the filter

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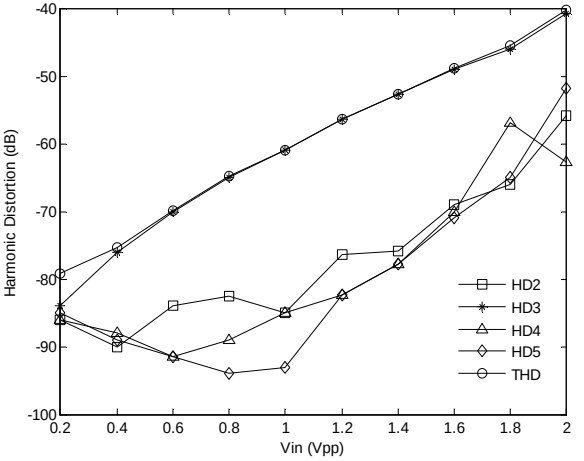

Figure 4.9. Measured harmonic distortion versus input amplitude

The tuning capability of the filter is seen in Figure 4.10, where the -3dB cutoff frequency measured for different frequency tuning voltages V_{tun1} is shown. As expected from (4.2) tuning is not linear; it depends inversely on V_{tun1}. It can be observed that the -3dB cutoff frequency range goes from 200 kHz to 1.5 MHz. This feature, together with the linearity achieved, makes the filter able to compensate for process and temperature variations and to be used in a dual-mode Bluetooth/ZigBee receiver.

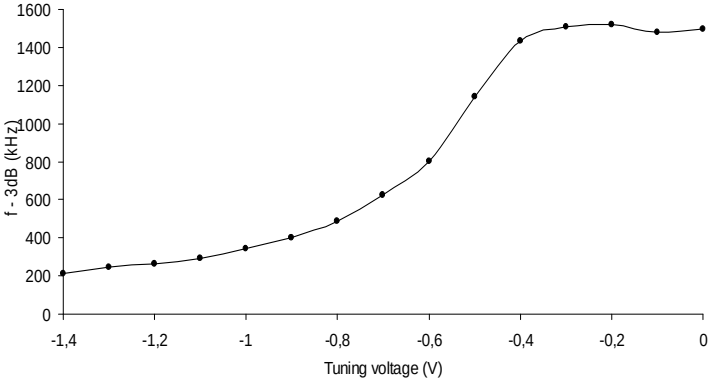

Figure 4.10. Frequency tuning of the filter

Figure 4.11 shows the measured frequency response of the filter for a cutoff frequency of 650 kHz (Bluetooth mode) and 1.2 MHz (Zigbee mode). The

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low DC gain value obtained in the measurement is due to attenuation introduced by the measurement setup. The behavior above 4 MHz is attributed to the input signal feedthrough in the test board.

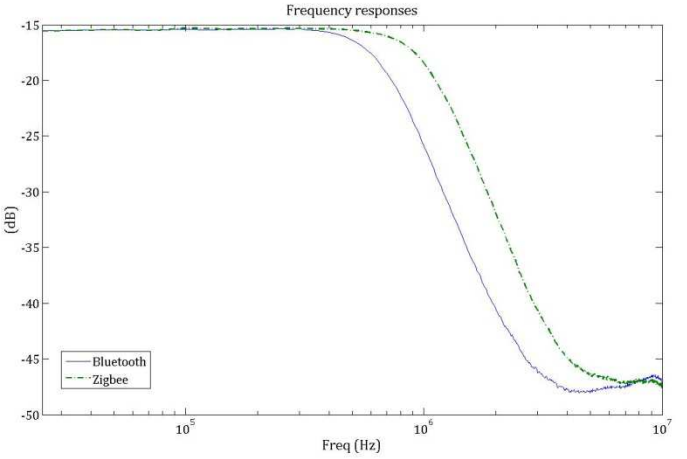

Figure 4.11. Measured frequency response of the filter

Figure 4.12 shows the measured filter Common-Mode Rejection Ratio (CMRR) versus frequency. Note that CMRR values range from 45 to 52 dB in the passband.

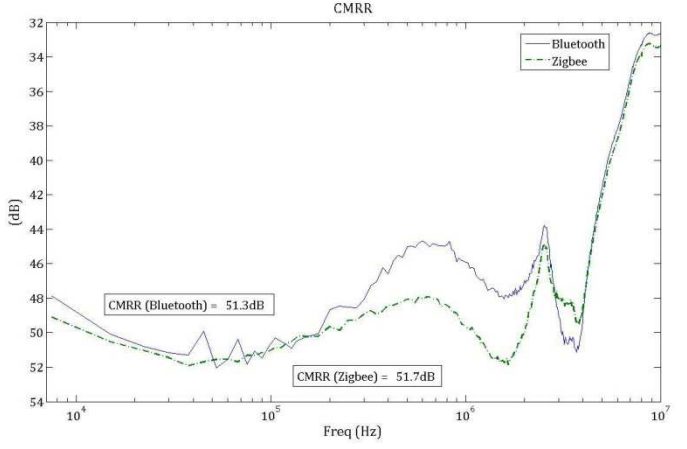

Figure 4.12. Measured CMRR versus frequency

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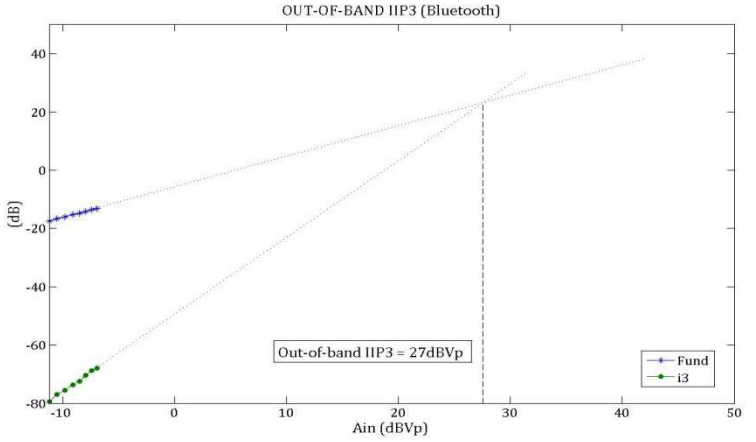
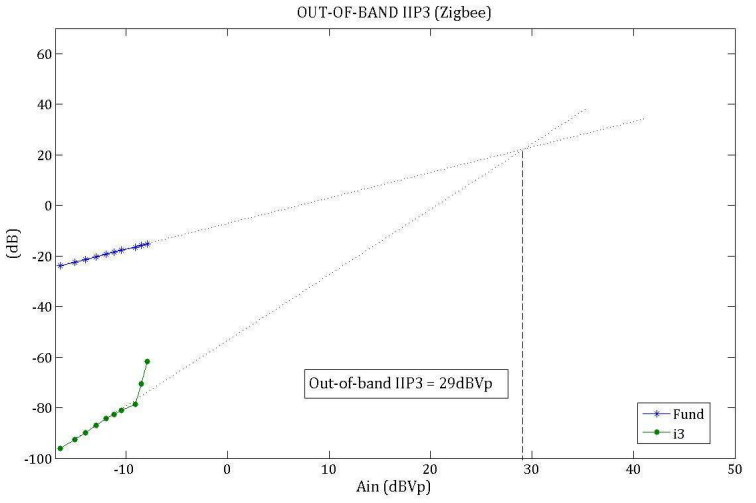
The measured out-of band IIP3 for Bluetooth and Zigbee modes is shown in Figure 4.13. The resulting values are 27 dBVp and 29 dBVp, respectively. For the Bluetooth mode, where the cutoff frequency is 650 kHz, the input tones were set to 2.4 MHz and 0.8 MHz. For the Zigbee mode, where the cutoff frequency is set to approximately 1.2 MHz, the input tones were of 1.7 MHz and 1.3 MHz.



(a)



(b)

Figure 4.13. Measured out-of-band IIP3 (a) Bluetooth mode (b) Zigbee mode

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Table 4.4 summarizes the main measured performance parameters of the filter for Bluetooth and Zigbee modes. Note that the proposed implementation fits the specifications in Table 4.1.

Table 4.4. Summary of Filter Measurement Results

Parameter	Value	
Filter Response	Butterworth	
Filter Order	3rd	
Technology	0.5µm CMOS	
Supply Voltage	±1.65 V	
Bias Current	10 µA	
Supply current (I_{DD})	1.4 mA	
Die area	2.22 mm^2	
Cutoff frequency range	200kHz-1.5MHz	
Mode	**Bluetooth**	**Zigbee**
Bandwidth (F_{-3dB})	650 kHz	1.2 MHz
Gain (A_0)	2.3 dB	3.2 dB
IIP3 (In-band)	23.5 dBVp	26 dBVp
IIP3 (Out-of-band)	27 dBVp	29 dBVp
Output Offset Voltage	<15 mV	<15mV
THD @ 1Vpp, 120 kHz	-55 dB	-60 dB
Input 1dB Compression	-20 dBVp	-20 dBVp
CMRR @ 200 kHz	51.3 dB	51.7 dB
PSRR+ @ 125 kHz	59 dB	59 dB
PSRR- @ 125 kHz	53 dB	53 dB
Eq. input RMS noise	185 µV	260 µV

Comparison between the proposed Gm-C tunable filter and previously reported ones [3–5], [18], [22–48] is shown in Figure 4.14. To this aim the following Figure of Merit (FoM) is employed:

$$FoM = \frac{Power\ per\ pole}{(Cutoff\ frequency) \cdot SFDR} \qquad (4.7)$$

where the Spurious-Free Dynamic Range (SFDR) of the filter is calculated as SFDR=$(IIP3/P_n)^{2/3}$, with P_n the input-referred noise power. To calculate the FoM in references where the IIP3 is not reported, IIP3 has been estimated from the IM3.

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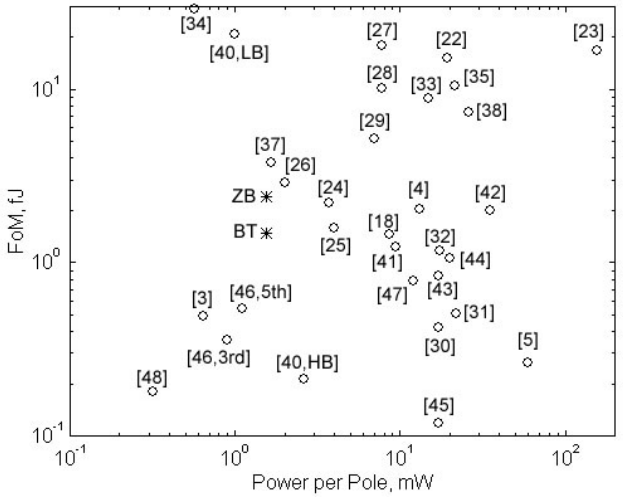
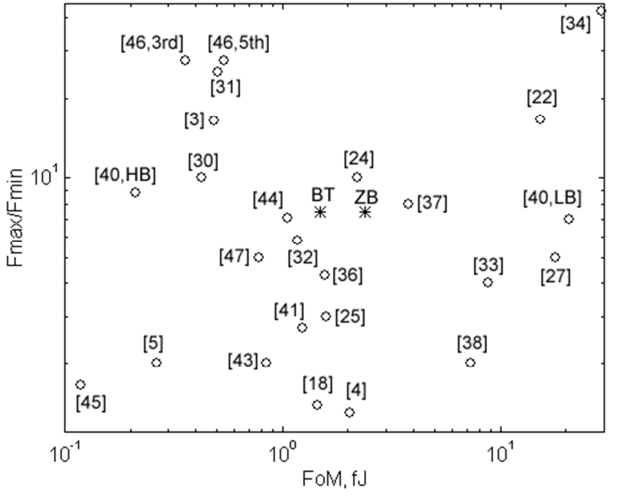


(a)



(b)

Figure 4.14. Filter performance comparison (a) FoM versus Power per Pole (b) Tuning ratio versus FoM

In Figure 4.14(a) this FoM is shown versus the power per pole. The fabricated filter is configured in Bluetooth mode (BT) with a cutoff frequency of 650 kHz, and in ZigBee mode (ZB) with a cutoff frequency of 1.2 MHz. The resulting value is shown with an asterisk in the graph, while the values

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corresponding to published references are shown with circles. It can be noticed that despite the relatively old technology employed, this work is comparable to remarkable achievements proposed to date. In Figure 4.14(b) the ratio between the maximum and minimum cutoff frequency is plotted versus the FoM. It can be noticed again that this work also compares favorably in this framework. Filters with a tuning ratio Fmax/Fmin > 10 usually employ a combination of discrete and continuous tuning.

To conclude this section, a novel wide range tunable highly linear third order low-pass G_m-C filter has been introduced. Low quiescent power consumption has been achieved thanks to the programmable transconductors operating in class AB employed for its implementation. Quasi-floating gate transistors have been used in order to obtain this class AB operation. As a result, the circuit features high current driving capability and, at the same time, very low quiescent power consumption. Besides, each transconductor of the filter includes in its design a technique for tuning the transconductance. This allows adjustment of the cutoff frequency as well as the quality factor of the filter. Finally, measurement results show a current consumption of 1.4mA, a tuning range of about four octaves and a THD < -50 dB for 120 kHz inputs up to 1.6 Vpp. These features make it useful for channel filtering of highly integrated, low power, multi-standard direct conversion wireless receivers.

4.3 Design of Channel Selection Filters for Bluetooth (2)

After the previous study, it is evident that the topology presented fulfills the requirements needed in the target applications. However, some improvements can still be done in the circuit in order to optimize the area employed or to adapt it better to wireless receivers necessities. This section is focused on explaining the addition of these improvements to the implemented filter.

4.3.1 Simplification of the Topology

Considering power consumption, although it cannot be said that it is very high in this specific filter comparing it with other low-pass filters found in literature, it should be reduced. In fact, according to Figure 4.14(a) where the filter is shown in the middle of the figure when the FoM is represented versus the Power per Pole, it can be concluded that the power consumption must be reduced in order to make it a more suitable option for a receiver.

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There are different possibilities to reduce the power consumption of the circuit, such as reducing its bias current. Note however that a decrease in the bias current means also linearity deterioration, so a tradeoff must be found between consumption and distortion. Another useful approach is based on simplifying the topology, as less components and branches imply less power consumption. Moreover, Figure 4.8 showed that the filter employs quite a considerable area, and it would be reduced also by simplifying the filter.

The filter described in Section 4.2 employs just three CMFB circuits for its six transconductors because the outputs are shared between them, as Figure 4.3 illustrates. Due to that same reason, the output CCII of the transconductors, those that act as current followers (CCII 3 and 4 of Figure 4.5), could be shared as well, allowing an optimization of the circuit by eliminating unnecessary buffers. These circuits are just in charge of carrying the current from a low-impedance output to a high-impedance one but they do not control the amount of current that flows through the output. As a consequence, the six different transconductors could just be composed of the non-tunable transconductor cores plus the current dividers implemented by triode transistors (CCII 1 and 2, passive resistors and current divider of Figure 4.5), and their outputs could be connected to a pair of CCII, acting as current followers, shared with other transconductors. This idea is illustrated in Figure 4.15.

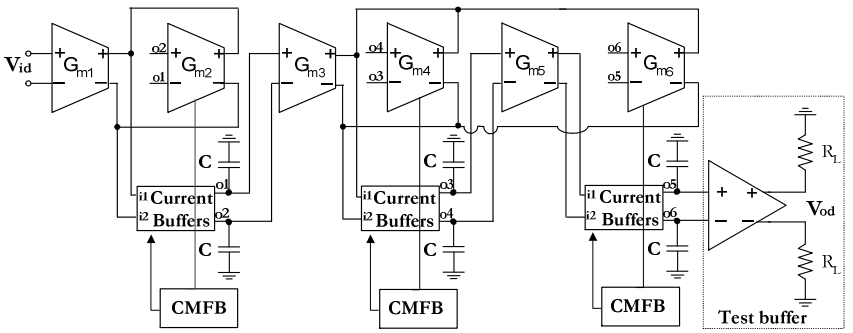

Figure 4.15. Simplified third-order Butterworth Gm-C channel filter

The symbol for the transconductor is still the same as in Figure 4.3, but this time its diagram is not the one shown in Figure 4.5. The diagram for these transconductors is depicted in Figure 4.16, while Figure 4.17 shows the schematic that corresponds to the block named Current Buffers. With this simplification, instead of a block Buffers for each transconductor, just half the blocks are needed for the complete circuit.

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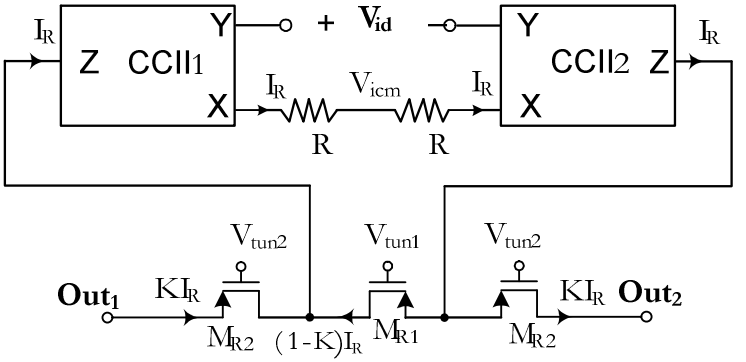

Figure 4.16. Simplified Transconductor Diagram

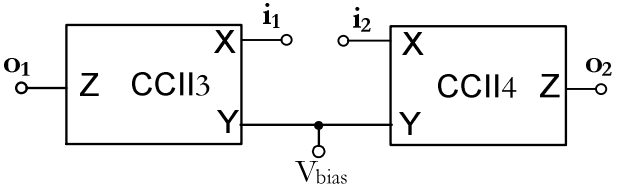

Figure 4.17. Shared Buffers

The performance of this filter is similar to that of the filter of Section 4.2, but an improvement in area, 35% less of area employed, and power consumption, 20% less of power consumption, has taken place.

Table 4.5. Comparison of Filters

	Original Filter	Simplified Filter
Area	2.22 mm^2	1.44 mm^2
Power Consumption	3.6 mW	2.9 mW

For that reason, this simplified version of the filter is going to be employed from now on.

4.3.2 Commutation between BT and ZB modes

It is interesting to design a versatile filter, useful for different standards or systems. A summary of the specifications required for several communications standards is presented in Table 4.6, obtained from [2], [25], [41], [46], [49–51].

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Table 4.6. Analog Baseband Filter Typical Specifications for Several Communications Standards in Zero-IF Receivers

Parameter	GSM Spec	Bluetooth Spec	CDMA2000 Spec	W-CDMA Spec	Zigbee Spec
Power	3.5mW	10mW	7mW	10mW	5mW
Filter order	3rd order	3rd/4th order	3rd/5th order	3rd/5th order	3rd/5th order
Cutoff freq.	f_c =115 kHz	f_c =650 kHz	f_c =700 kHz	f_c =2.2 MHz	f_c =1.2 MHz
IIP3	+10dBVp	+18dBVp	+15dBVp	+0dBVp	+10dBVp
$Noise_{output}$ PSD	400nV/√Hz	225nV/√Hz	200nV/√Hz	350nV/√Hz	250nV/√Hz

According to the frequency response and the cutoff frequency range obtained by measuring the original filter, it was more focused for Bluetooth. However, by doing some simple modifications, the filter can be suitable for using it either with Bluetooth or Zigbee, a very popular and widely employed standard nowadays. In order to use the filter with Zigbee, the frequency range needs to be moved an octave, allowing achieving with the same tuning voltage twice the frequency than in Bluetooth. To do that, there are two possibilities, either reducing to half the value of the capacitors or the value of the passive resistors. Obviously, once the filter is designed and implemented inside a chip neither the value of the capacitors nor the value of the passive resistors can be changed. Therefore, it is necessary a switch that allows selecting a specific value for these components and, as a consequence, a specific frequency range, making the filter more suitable for one standard or the other.

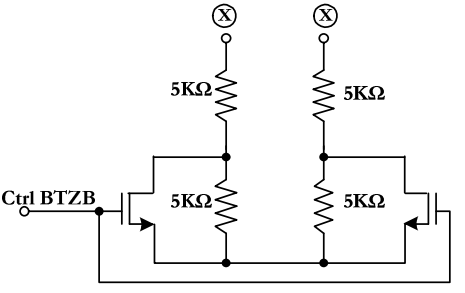

Figure 4.18. Switch BT/ZB

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The simple switch that has been added to the design can be found in Figure 4.18. Of course, the X terminals connected to the resistors correspond to the X terminals of the first two CCII of the transconductor employed to implement the filter.

When $Ctrl_{BTZB}$ has a value of V_{DD}, there is current through the transistors (W/L = 200µ/0.6µ), their resistance decrease, and they behave as short circuits, dominating over the passive resistors because they are in parallel. As a result, the total resistance is 10kΩ, which corresponds to the Zigbee configuration. However, when $Ctrl_{BTZB}$ has a value of V_{SS}, there is no current through the transistors, they behave as open circuits, and the total resistance is 20kΩ, suitable for Bluetooth.

This switch must be included in each transconductor of Figure 4.15 in order to improve the design and adapt it better to current trends. A simulation of the frequency response of the filter is shown in Figure 4.19, where the control signal $Ctrl_{BTZB}$ has been set to two values, V_{DD} and V_{SS}. It can be clearly seen how the cutoff frequency range has moved, being almost twice for Zigbee than for Bluetooth.

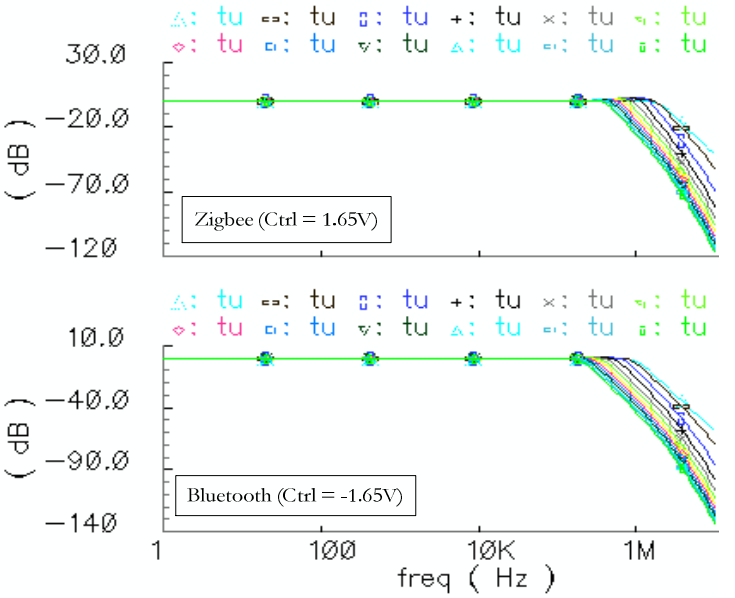

Figure 4.19. Frequency response by switching BT/ZB

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4.3.3 Tuning Control

Designing an Automatic Tuning Circuit for the filter would mean also a great improvement and, in fact, is almost essential because, from a commercial point of view, it is unfeasible to design a filter in which the cutoff frequency needs to be tuned manually each time. In order to control the auto-tuning of the circuit either some external elements are employed, like capacitors or resistors, or an external reference signal is needed, a clock or sinusoidal one of which frequency sets the nominal frequency of the filter, like this case. The first approach is usually done when on-chip tuning is made only once, typically after fabrication. The second one is more convenient when programmability of the filter characteristics is required, as it can be easily achieved by changing the reference signal. In our proposal, by changing the frequency of the new circuit, the cutoff frequency of the original filter can be tuned, achieving like that a master-slave configuration, where the new circuit and the original filter are the master and the slave, respectively.

There are different possibilities to implement an automatic tuning system for a filter but, among them, two configurations have been chosen to be implemented in this work. This Section is focused on studying a tuning circuit based on analogue squarer circuits, and another one that makes use of peak detectors.

4.3.3.1 General Tuning System

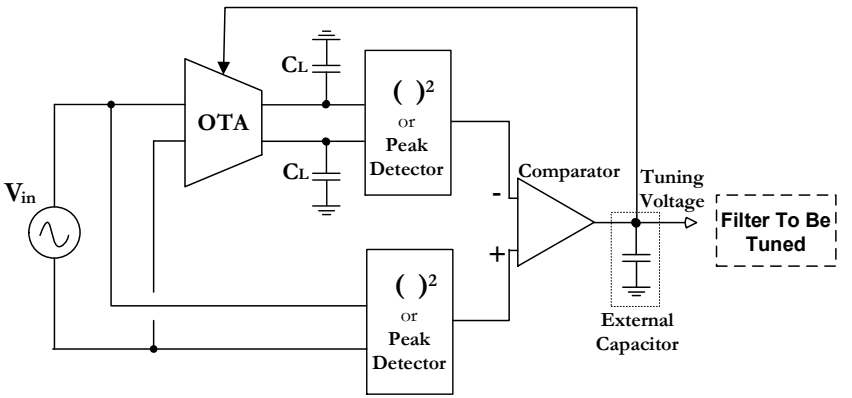

Figure 4.20. Automatic Frequency-Tuning System

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The on-chip automatic tuning system chosen as starting point is the one presented in [18]. It is based on a G_m-C integrator using the same transconductor as in the main filter, tuned using a negative feedback loop. It is a simple model taking into account that the OTA or transconductor has been already implemented in the filter, Figure 4.5, and can be reused in here. The diagram of the circuit is shown in Figure 4.20.

The integrator's unity-gain frequency is given by

$$f_u = \frac{G_m}{2\pi C_L} \qquad (4.8)$$

where G_m is the overall OTA small-signal transconductance. By applying a reference signal $V_{ref} = V\sin(2\pi f_r t)$, the integrator output voltage becomes

$$V_o = \frac{G_m}{C_L}\int V_{ref}\,dt = \left(\frac{f_u}{f_r}\right)V\cos(2\pi f_r t) \qquad (4.9)$$

Note that the integrator's output is proportional to the ratio of the unity-gain frequency to the reference frequency. Hence, comparing the amplitude of the integrator's output and that of the reference signal (V), the integrator unity gain frequency can be locked to the reference frequency. If f_r changes, f_u must change as well in order to keep both amplitudes equal. As C_L remains constant, according to (4.8), a change in f_u means a change in G_m. Consequently, the tuning voltage of the transconductor will change as well as the cutoff frequency of the filter.

As it has been said, the voltage level comparison can be realized using two peak detectors or two squarer circuits. Using an external capacitor of 3 nF (its exact value is not critical), the high-frequency signals are rejected. An additional CMFB circuit reduces the OTA common-mode dc offset.

4.3.3.2 Tuning with Squarer Circuits

The first approach is based on the comparison of the mean squared values of the signals. Squaring V_{ref} and V_o and applying well-known trigonometrical identities, the following expressions can be obtained:

$$V_{ref}^2 = \frac{V^2}{2} - \frac{V^2}{2}\cos(4\pi f_r t) \qquad (4.10)$$

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$$V_o^2 = \frac{V^2}{2}\left(\frac{f_u}{f_r}\right)^2 - \frac{1}{2}\left(\frac{f_u}{f_r}\right)^2 V^2 cos(4\pi f_r t) \qquad (4.11)$$

After filtering out the high-frequency components, the dc levels are compared to obtain the correction error. This error is used to adjust f_u by tuning G_m through the gate voltage of the triode-biased transistors. If the control-loop dc gain is large enough, under steady-state conditions the error is close to zero and G_m/C_L is tuned to the reference frequency.

The squarer chosen for the scheme has been previously proposed in [52], [53]. The exact diagram employed in this work is illustrated in Figure 4.21 and its transistors aspect ratios are provided in Table 4.7. It is a good choice because of its simplicity, low supply requirements and its class AB operation, which is interesting because the filter also operates in class AB.

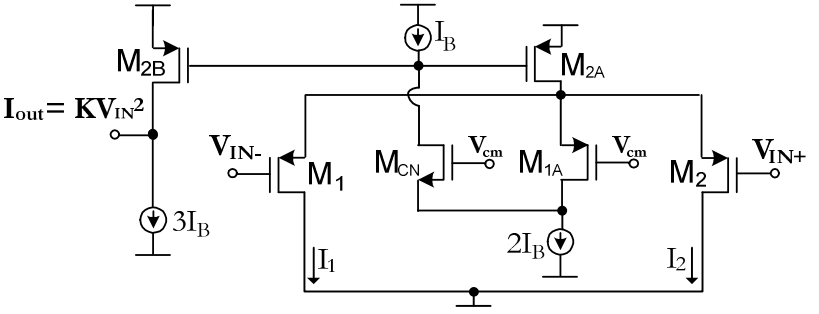

Figure 4.21. Squarer Circuit

In this circuit, when a differential input $V_{id} = V_{in+} - V_{in-}$ is applied, complementary gate-source voltage changes with values $V_{id}/2$ and $-V_{id}/2$ appear in M_2 and M_1, respectively. This leads to an imbalance in the drain currents that is not limited by the quiescent current. Currents I_1 and I_2 are given by

$$I_1 = \frac{\beta_{1,2}}{2}\left(V_B + \frac{V_{id}}{2}\right)^2 \qquad (4.12)$$

$$I_2 = \frac{\beta_{1,2}}{2}\left(V_B - \frac{V_{id}}{2}\right)^2 \qquad (4.13)$$

where $\beta_{1,2} = \mu_n C_{ox}(W/L)_{M1,2}$ is the transconductance factor of transistors M_1 and M_2. Hence $I_1 + I_2 = \beta_{1,2} V_B^2 + (\beta_{1,2}/4)V_{id}^2$ leading to the required square law. This implementation of the squarer circuit is based on noting that the sum of

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currents I_1+I_2 is already present in transistor M_{2A}. This topology features a large input range and is well suited for low supply voltage, as mentioned above.

Table 4.7. Transistor Aspect Ratios

Transistor	Value (µm/ µm)
M_1, M_2, M_{1A}, M_{cn}	50/1.2
M_{2A}, M_{2B}	400/1.2

Figure 4.22 shows the complete tuning system implemented with squarer circuits. The blocks have been already explained. A CMFB has been added, not only to control the common mode but also to provide the V_{cm} voltage needed at the squarers, and a current mirror has been placed at the output of one of the squarers (W/L = 300µ/15µ). Since the squarer output signal is current, a simple current mirror is enough to carry out the above-mentioned current comparison, by changing an output current direction so that a subtraction of both outputs can take place. The resulting current is low-pass filtered by the external capacitor and used to tune the OTA and the slave filter.

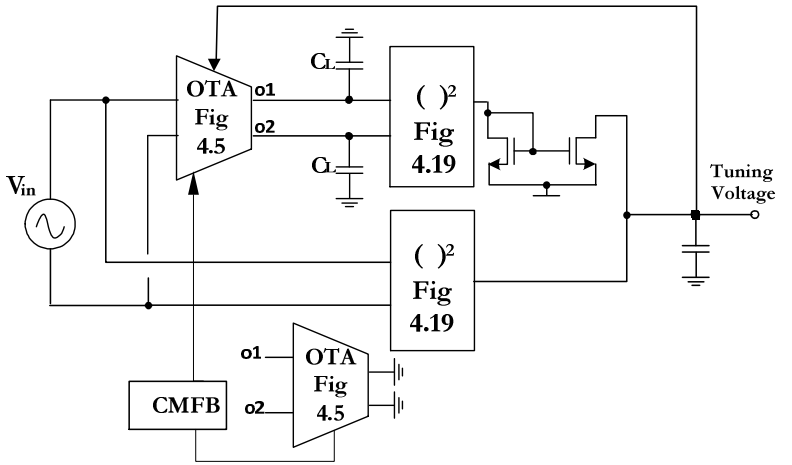

Figure 4.22. Automatic Tuning System with Squarers

Figure 4.23 shows a simulation of different reference frequencies, illustrating the input (middle) and output voltage (top) of the integrator, as well as the resulting Tuning Voltage (bottom). Note that the tuning voltage stabilizes when both voltages achieve the same amplitude.

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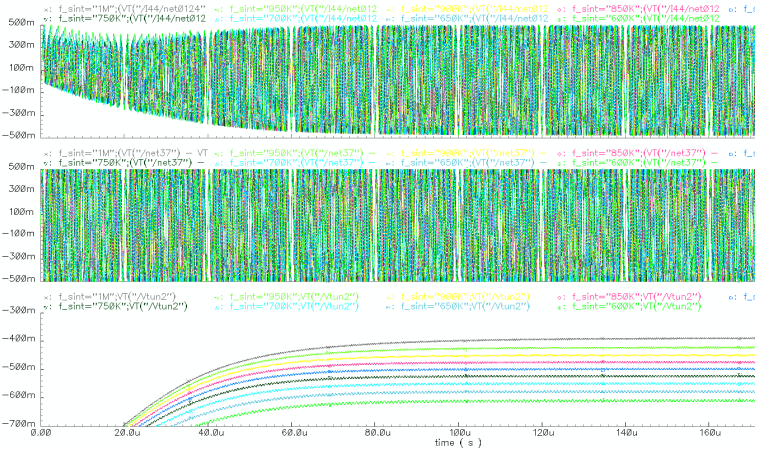

Figure 4.23. Tuning Voltage with Squarers

In order to prove the proper performance of the automatic tuning system along with the filter, another simulation has been done. By changing the reference frequency of the input of the automatic tuning system (V_{in} = $1V_{pp}$), the output tuning voltage that goes to the OTA and to the filter, once stabilized, takes different values and, consequently, the cutoff frequency of the filter changes among the values of its range. As the tuning voltage is now a transient signal, different frequencies of the input signal of the filter need to be tried in order to find the -3dB cutoff one (until the value of the output amplitude of the filter is 0.71 times the value of the input one). The results obtained for Bluetooth, i.e. for a total resistance of 20kΩ to do the V-I conversion, are shown in Table 4.8.

Table 4.8. Simulation Results for BT

f_ref	Tuning Voltage	fc -3dB
200 kHz	-1.43 V	260 kHz
300 kHz	-1.03 V	400 kHz
400 kHz	-814 mV	570 kHz
500 kHz	-691 mV	750 kHz
600 kHz	-609 mV	940 kHz
700 kHz	-548 mV	1.08 MHz
800 kHz	-497 mV	1.11 MHz
900 kHz	-448 mV	1.12 MHz
1 MHz	-388 mV	1.12 MHz
1.1 MHz	-256 mV	1.12 MHz

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As it can be seen, the complete system works properly. The frequency range is almost similar to the one obtained with the original filter without the automatic tuning system. Note that the middle frequency of the range is approximately 650 kHz, just what is necessary for Bluetooth. Applying this same simulation for Zigbee, for the same reference frequencies, the cutoff ones are doubled.

4.3.3.3 Tuning with Peak Detectors

The second approach is based on employing peak detectors instead of squarers before comparing the output signals. The proposed frequency tuning circuit based on peak detection method is a version of Figure 4.20.

The peak detectors consist of full- or half-wave rectifiers with discharge resistors and capacitors and they are employed to detect the peaks of the input and output voltage of the integrator. The comparator is used to determine the signal difference between the outputs of the two peak detectors. The external capacitor holds the output signal of the comparator, which is connected to the tuning node of the transconductance G_m. If the input signal V_i of the integrator is a sine wave with frequency equal to the cutoff frequency of the to-be-tuned lowpass filter, the gain of the integrator is unity and the magnitude of the integrator output will ideally be the same as the magnitude of the input voltage [54].

The phase between them differs by 90º. The magnitudes of the peak detector outputs are the same. Hence, the output voltage of the comparator is half of the power supply voltage and is set to be the desired tuning voltage. Because the OTA, peak detector, and comparator form a negative feedback loop, the high gain of the comparator eventually will generate a proper tuning voltage, to equalize the outputs of the peak detectors. The same tuning voltage is applied to the lowpass filter to tune it to the desired cutoff frequency.

The peak detector chosen for this implementation has been presented in [55]. The schematic is illustrated in Figure 4.24 and Table 4.9 shows the transistors aspect ratios.

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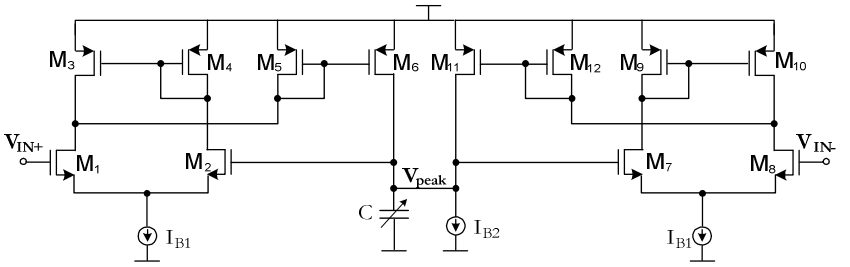

Figure 4.24. Peak Detector

As it is shown in the figure, a positive peak detector is constructed with a differential amplifier ($M_1 \sim M_4$) and a current mirror (M_5 and M_6). If the V_{in} is larger than the V_{peak}, the excess current is flowing through M_5 which is also copied to M_6 and charging the hold capacitor C. The small current source I_{b2} is for discharging. On the contrary, if V_{in} is smaller than V_{peak}, there is no current flowing through M_5 and M_6, and the capacitor is going to hold its value. The droop rate of the peak detector can be controlled by adjusting the values of the capacitance and the current source.

Table 4.9. Transistor Aspect Ratios

Transistor	Value (μm/ μm)
M_1, M_2, M_7, M_8	42/0.6
M_3, M_4, M_9, M_{10}	63/0.6
M_5, M_6, M_{11}, M_{12}	18/0.6

It is important to optimize the values of the hold capacitor and the current source to accurately detect the peak of a certain input signal. Therefore, it is difficult to make a peak detector work for a wide range of input frequencies. In order to design a peak detector for multistandard wireless receivers, the peak detector need to process a broader range of input signals. The differential configuration of the circuit allows achieving that. Both positive and negative differential input signals are fed to two identical positive peak detectors, and a hold capacitor and a current source are shared. The single-ended output peak voltage is thus the maximum of the two peak voltages. Here, to make it work for more than one wireless standard, the capacitor C can be made variable by using switches. In this work a capacitor of 8 pF has been employed.

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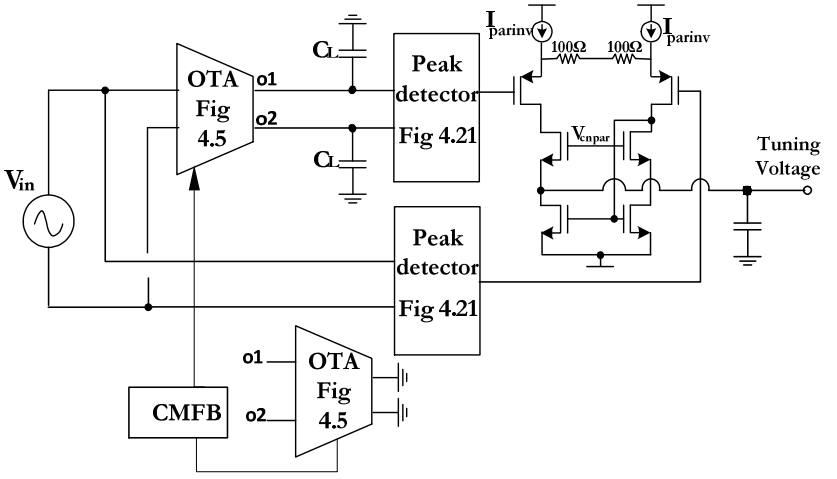

Figure 4.25. Automatic Tuning System with Peak Detectors

The complete tuning system implemented with peak detectors is shown in Figure 4.25. The blocks have been already described, the CMFB circuit has been added like in the previous topology, and the outputs of the peak detectors, being voltages, have been connected to a subtraction circuit.

Note that a high input impedance subtraction circuit is necessary at the output of the peak detectors, in order to avoid the outputs to be charged resistively, like this differential pair with resistive degeneration finally chosen. If the output of the first peak detector, the one after the integrator, is lower than the other one, the operation of the differential pair increases it, making both outputs equal again. If its gate voltage is lower, the top left transistor is going to drive more current than the opposite one and, having a current mirror at the bottom, the extra current is going to be eliminated through the capacitor, charging it and, consequently, increasing the tune voltage. An increase in the tune voltage means an increase in the output current of the integrator, and in the output voltage as well. The tune voltage is going to keep rising until both outputs of the peak detectors become equal.

As in the previous system, Figure 4.26 shows a simulation of different reference frequencies, illustrating the input (top) and output voltage (middle) of the integrator, as well as the resulting Tuning Voltage (bottom). Again the tuning voltage stabilizes when both voltages achieve the same amplitude.

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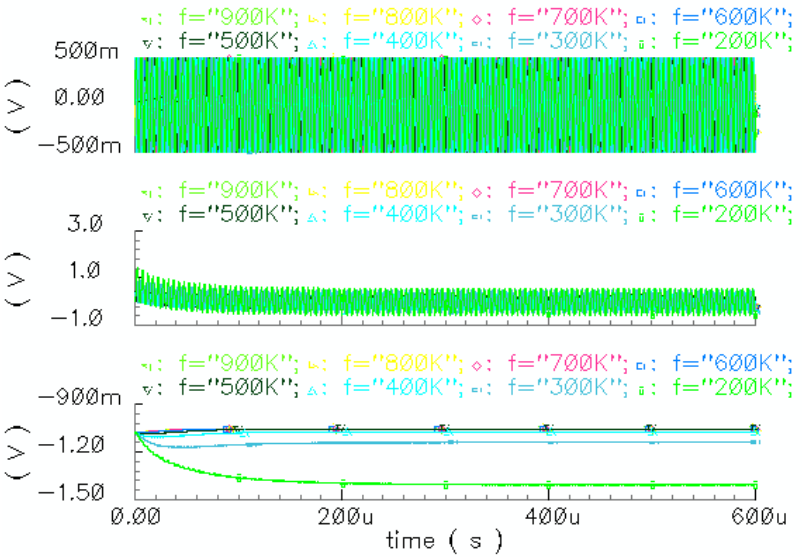

Figure 4.26. Tuning Voltage with Peak Detectors

Also as in the squarers case, to prove the proper performance of the automatic tuning system along with the filter the same simulation has been done. By changing the reference frequency, the output tuning voltage takes different values and, consequently, the cutoff frequency of the filter changes among the values of its range. The results obtained for Bluetooth are shown in Table 4.10.

Table 4.10. Simulation Results for BT

f_ref	Tune Voltage	fc -3dB
200 kHz	-1.4 V	270 kHz
300 kHz	-1.08 V	375 kHz
400 kHz	-910 mV	480 kHz
500 kHz	-800 mV	585 kHz
600 kHz	-704 mV	735 kHz
700 kHz	-616 mV	930 kHz
800 kHz	-568 mV	1.05 MHz
900 kHz	-520 mV	1.13 MHz
1 MHz	-455 mV	1.13 MHz

In this case, a frequency range that goes from 270 kHz to 1.13 MHz has been obtained, so again is suitable for Bluetooth. As before, by applying this same

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simulation for Zigbee, for the same reference frequencies doubled cutoff frequencies are achieved.

4.3.3.4 Comparison Squarers vs Peak Detectors

Besides Tables 4.7 and 4.9, that already show performance differences between both systems, some simulations have been done in order to do a better comparison, like these of the following figures.

Figure 4.27 shows the tuning voltage obtained with the two tuning systems when a transition in the input voltage takes place. Two tones of 500 mV_{pp} and 500 kHz (f_ref), one of them with a delay of 200µs, have been employed as an input. Note that both approaches achieve approximately the same tuning voltage and react in a similar way to the transition, being the stabilization time almost the same.

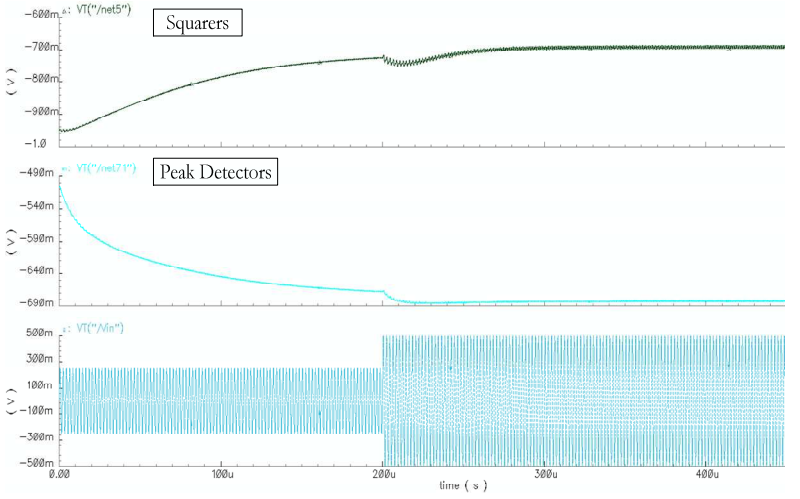

Figure 4.27. Transition between two tones of 500 mV_{pp}

In Figure 4.28 the tuning voltage of both systems has been obtained for different reference frequencies. The frequencies employed have been 100k, 200k, 500k, 800k and 1MHz, and their corresponding tuning voltages go from bottom to top respectively. It can be noticed that, with peak detectors, the signals have less ripple but, on the other hand, with the squarers, the tuning voltage settles to its stabilized value faster. Both are good systems so, depending on what they look for, the designers should choose one or the other.

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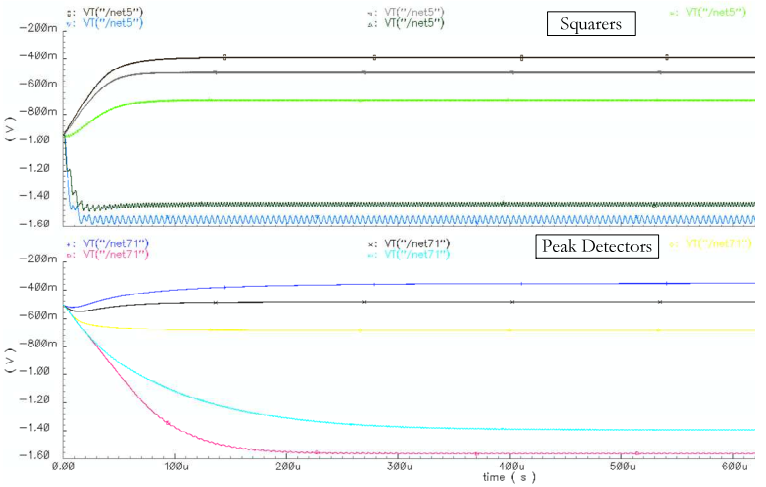

Figure 4.28. One tone of 500 mV_p and different f_ref

Both explained automatic tuning systems have been fabricated along with the improved filter in a standard 0.5µm CMOS n-well process with nominal nMOS and pMOS threshold voltages of 0.64 V and –0.92 V respectively. The microphotograph of the circuit can be seen in Figure 4.29. It must be highlighted that in the same area occupied by the original filter, now the improved filter as well as two automatic tuning systems can be found.

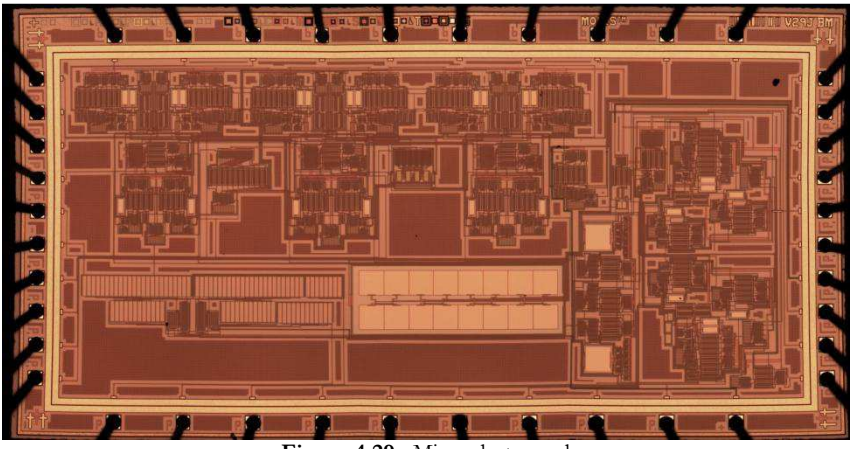

Figure 4.29. Microphotograph

Some experimental measurements must be done in order to check if the performance of the circuit is similar to the simulation results. Unfortunately, the

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fabricated chip just arrived when this thesis was almost finished, so there was not enough time to do the measurements. This constitutes necessarily a future line of work.

4.4 Summary

A novel wide range tunable highly linear third order low-pass G_m-C filter has been introduced in this Chapter. Low quiescent power consumption has been achieved thanks to the programmable transconductors operating in class AB employed for its implementation. Quasi-floating gate transistors have been used in order to obtain this class AB operation. As a result, the circuit features high current driving capability and, at the same time, very low quiescent power consumption. Besides, each transconductor of the filter includes in its design a technique for tuning the transconductance. This allows adjustment of the cutoff frequency as well as the quality factor of the filter. As a result, this circuit is useful for channel filtering of highly integrated, low power, multi-standard direct conversion wireless receivers.

The second part of the chapter has been focused on improving the original circuit, by eliminating unnecessary components or adding extra elements. Moreover, two automatic tuning systems have been implemented in order to adapt the filter to current necessities.

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CHAPTER 5

Other applications of class AB transconductors

Besides their use in channel-selection filters for wireless receivers, like the one implemented in Chapter 4, the highly-linear transconductors that have been proposed in this work are useful for many other applications. The aim of this chapter is showing some of them, like the design of an amplifier with variable gain (VGA) and gain-independent bandwidth.

Variable Gain Amplifiers are required in several applications such as medical equipment, telecommunication systems or disk drives, allowing maximization of the dynamic range. Their use in wireless receivers is critical since the signal power strength at the receiver input can vary significantly. A VGA is typically employed in a feedback or feedforward loop arrangement to form an automatic gain control (AGC) system that detects the input signal level and adjusts the gain to obtain an almost constant signal level at the output, improving the operation of the subsequent stages of the receiver. It is important to achieve gain values with exponential dependence on the control signal because this feature allows linear-in-dB gain setting and minimizes the settling time of AGCs.

From the control signal point of view, there are two basic approaches in the realization of VGAs. With a digital control signal [1], the gain can be varied discretely using, for example, an array of switchable passive resistors as shown in Figure 5.1(a). When the gain must be set more accurately a continuous control is needed, like the one in Figure 5.1(b). In this case, an analog signal can be used to

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change, for example, transconductance characteristics or active resistors, but to achieve an exponential gain variation with the control signal is not trivial and several techniques can be used [2–4]. A combination of both methods [5] is also possible to get a wider gain range without losing the continuous tuning capability. In communications, typically continuous-type VGAs are preferred to avoid signal phase discontinuities.

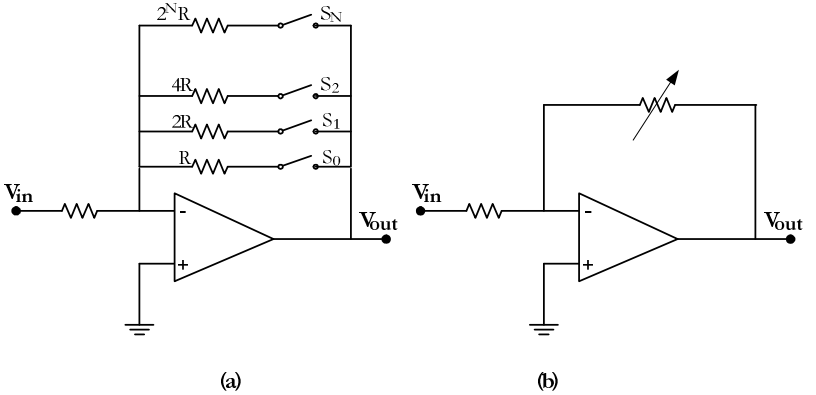

Figure 5.1. Basic control schemes for VGAs (a) Digital control (b) Analog control

Conventional amplifier structures suffer from the common gain-bandwidth conflict which is one of the most critical limitations in analog electronics. In VGAs, this limitation implies that the bandwidth reduces as the gain increases. This could be a serious issue in several applications. Some solutions have been reported to solve this problem [6] and to achieve a constant bandwidth operation. Besides, power consumption is another critical issue in low-power applications such as wireless transceivers in autonomous wireless sensor nodes. Conventional VGAs often operate in class A, so the maximum signal current is limited by the quiescent current. In low power applications such as low power wireless receivers, a class AB implementation of the VGA is advantageous in order to achieve proper dynamic performance with low quiescent currents [7].

In this chapter, a novel design for a VGA with constant and maximum bandwidth is going to be presented. The design allows continuous gain variation using a two-stage class AB structure with a programmable transconductor, the one proposed in the previous chapter [8], and a class AB transresistance amplifier.

This Chapter is organized as follows. Section I describes the Cherry-Hooper Circuit, on which the designs of this Chapter are based. The

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implementation of a one-stage Variable Gain Amplifier is covered in Section II, achieving at the end of it a novel circuit with simulation and measurement results. In Section III some modifications to the previous design are made, in order to improve it, like adding more stages to the circuit. Finally, conclusions are given in Section IV.

5.1 Variable Gain Amplifier: Cherry-Hooper Circuit

According to the well-known expression BW=GB/(1+|G|), where GB is the gain-bandwidth product of an op-amp, the conventional voltage feedback amplifier of Figure 5.2(a) has a bandwidth, BW, that is inversely proportional to the nominal closed-loop gain, $G=-R_F/R_I$. Moreover, it requires a low impedance source, i.e. buffered signal source with internal impedance $R_S<<R_I$, in order to avoid gain degradation or inaccurate gain when source impedance R_S is comparable to R_I. On the other hand, the conventional non-inverting amplifier with nominal gain $G=1+R_F/R_I$ does not require a buffered source, like the inverting one, but it has high common mode input swing and cannot be implemented in fully differential form, which is advisable in the designs that are being implemented along this work in order to reduce common mode noise in mixed signal VLSI systems and pair-order distortion [9].

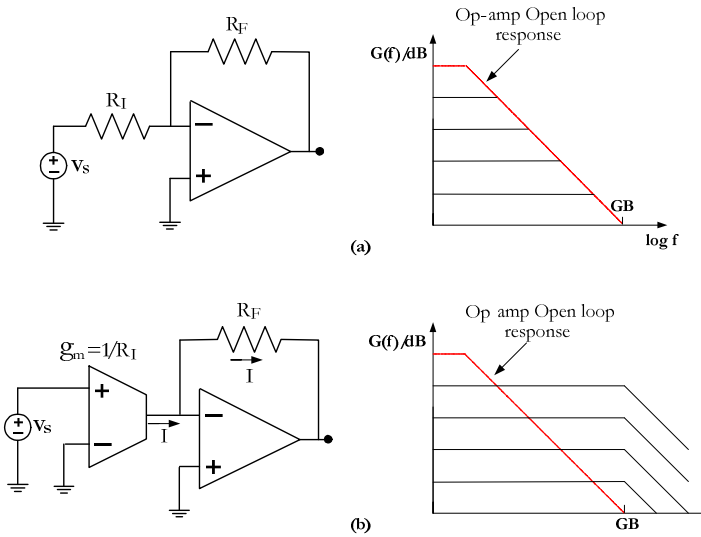

Figure 5.2. (a) Conventional op-amp amplifier with bandwidth reciprocal to gain (constant GB) (b) OTA-OP-amp amplifier with constant maximum bandwidth BW=GB independent of gain or of elements R_F, R_I.

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However, current applications demand amplifiers featuring constant bandwidth and programmable gain, like the one shown in Figure 5.2(b). This figure illustrates the combination of an OTA and a feedback op-amp acting as a transresistance amplifier, circuit that is based on the Cherry-Hooper amplifier [10] that allows designing highly-linear CMOS amplifiers with precise programmable gain and large bandwidth that remains constant regardless of the gain adjustment. The basic Cherry-Hooper amplifier is shown in Figure 5.3 [11]. The output of the OTA acts as a virtual ground, allowing the large bandwidth, and high-impedance requirements and large output swing for the OTA. Besides, if $R_F << R_I$, where R_I is the inverse of the OTA transconductance, the bandwidth of the amplifier is approximately GB.

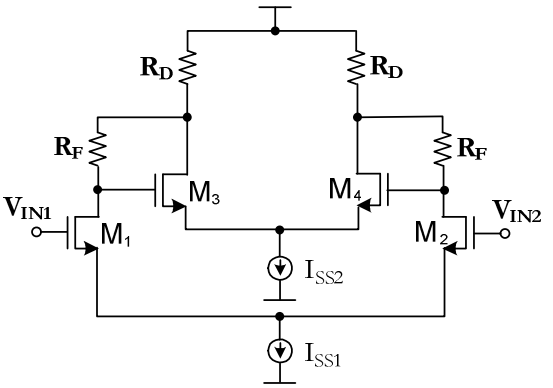

Figure 5.3. Standard MOS Cherry-Hooper Amplifier

Keeping this model in mind, several approaches have been reported that allow implementation of amplifiers with approximately constant bandwidth independent of the gain. The most common one is based on Current Feedback Operational Amplifiers (CFOAs)[12], which appear replacing the op-amp in the topology of Figure 5.2(a). Their inverting input terminal follows the voltage of the non-inverting input terminal, and their impedance, Zo, at the inverting input terminal must be very low (ideally zero). In practice the input stage of a CFOA is a voltage buffer connected between the positive and negative input terminals and its output impedance, Zo, corresponds to the input impedance of the inverting terminal of the CFOA. The bandwidth of an amplifier using CFOAs is given by $BW=1/[C_zR_F(1+Z_o/R_I)]$ [13] where C_z is the compensation capacitance of the CFOA. Feedback resistors R_F are maintained fixed and the gain is varied with R_I in order to maintain an approximately constant bandwidth, of value $BW=1/C_zR_F$, independent of gain. This is valid as long as gain is adjusted with R_I and the

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condition $|Z_o|<<R_I$ is satisfied over the amplifier's bandwidth and over the gain tuning range. While in bipolar technology it is easily satisfied, in CMOS technology it is difficult due to the output impedances of CMOS buffers that go from hundreds of Ωs to even kΩs. This leads to the fact that very low values for $|Z_o|$ over wide bandwidths can only be achieved at the expense of large silicon area (W/L) and large static power dissipation. By using shunt feedback in CMOS buffers to achieve very low values $|Z_o|$[14], $|Z_o|$ remains low only at low frequencies given that for stability reasons the loop gain of the buffer's shunt feedback loop must have a dominant pole and this causes the loop gain to decrease rapidly with frequency. As in the voltage feedback amplifier case, the fully differential version of a CFOA is only available as inverting amplifier and requires also a buffered signal source in order to avoid gain degradation.

5.2 One-Stage Variable Gain Amplifier

This section is focused on the implementation of a VGA with constant and maximum bandwidth, and continuous gain adjustment. As it has been said before, the design is going to employ a two-stage class AB structure with a programmable transconductor and a class AB transresistance amplifier. It is going to be based on the classical scheme of the Cherry-Hooper amplifier, taking the topology of Figure 5.2(b) as a model.

In this topology, an operational transconductance amplifier transforms the input voltage, V_s, into a current, $I=G_mV_s$, and then, this current is transformed by the transresistance amplifier into an output voltage, $V_{out}=-IR_F$. Therefore, the gain is given by $G=G_mR_F$. If the transconductance gain of the OTA is dependent on an internal resistor, R_I, then $G_m=1/R_I$ and the gain of the circuit is given also by $G=-R_F/R_I$.

5.2.1 Proposed VGA Scheme

The implementation of the VGA can be seen in Figure 5.4. As mentioned above, it is made by the cascade connection of a transconductor and a transresistance amplifier which allows gain-independent bandwidth [9], [10] since it does not depend on the transconductance of the first stage or the feedback resistance of the second stage. Besides, this topology allows both circuits to operate with maximum bandwidth due to the virtual ground that appears at the input of the amplifier and the high output impedance of the transconductor respectively. Moreover, thanks to that virtual ground that appears at the input of the transresistance amplifier, lower output impedance transconductor cells can be

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used. As a result, the output of the transconductor node is less sensitive to the effect of parasitic capacitances and noise.

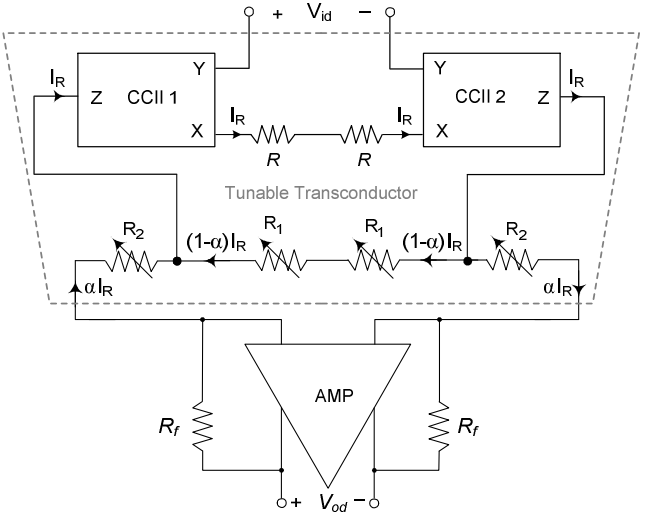

Figure 5.4. VGA implemented using the transconductor-transresistance scheme

5.2.1.1 Tunable Transconductor

The design of the transconductor is also shown in Figure 5.4. Needless to say that it is the same transconductor implemented in Chapter 4 to be employed in the channel selection filter. It was based on two second-generation current conveyors (CCIIs) [15] and two passive resistors in series. In Figure 5.5 the proposed transistor-level implementation of the CCII is reminded. As it has been previously explained, it is formed by a class AB voltage follower whose output current is conveyed to a high-impedance output node by replicating the output branch of the follower. Wide-swing cascode current mirrors and current sources have been employed. The explanation of the voltage follower block is not going to be repeated here, as it has been already covered in detail in Chapters 3 and 4.

Also illustrated in Figure 5.4, a tunable resistive divider placed at the Z outputs of the CCIIs has been chosen for continuous transconductance tuning [16] in order to achieve variable gain for the VGA. The output current of the resistive divider is finally applied to the transresistance amplifier with passive feedback resistors R_f.

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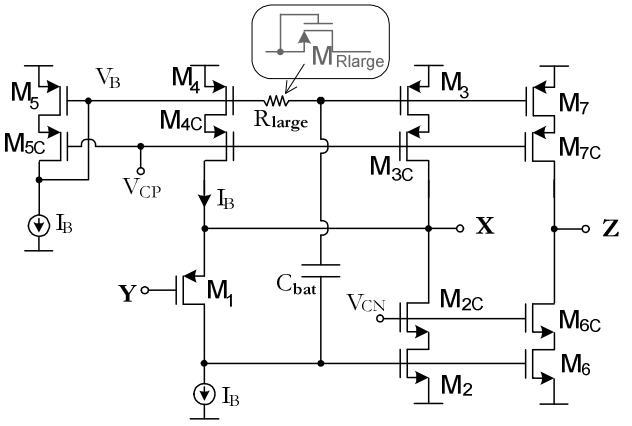

Figure 5.5. Class AB CCII

Regarding the mentioned continuous tuning method, as in the filter case, resistors R_1 and R_2 form a resistive divider, which controls the amount of current flowing to the transresistance amplifier, αI_R, where α is:

$$\alpha = \frac{1}{1 + R_2/R_1} \tag{5.1}$$

Consequently, the expression for transconductance is:

$$G_m = \frac{2\alpha I_R}{V_{id}} = \frac{\alpha}{R} \tag{5.2}$$

The current αI_R flowing through the second stage produces a VGA output voltage:

$$V_{od} = 2\alpha I_R R_f \tag{5.3}$$

Finally, from (5.2) and (5.3), the VGA gain becomes:

$$A_{CL} = \alpha \frac{R_f}{R} \tag{5.4}$$

which can be continuously adjusted by α ($\alpha \leq 1$) and hence by the value of R_1 and R_2 as (5.1) indicates. These resistors have been implemented with MOS transistors in the triode region that can be continuously tuned by changing their DC gate voltages $V_{tun1} = V_{tun3}$ and V_{tun2}. Despite the use of active resistors

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linearity is high, since passive resistors are still used for V-I conversion. Triode transistors are just used for current splitting.

5.2.1.2 Transresistance Amplifier

The second stage of the VGA is a class AB transresistance amplifier, as it has been shown in Figure 5.4. The transistor-level implementation of this circuit is shown in Figure 5.6. A VGA with a differential topology will be formed by two identical single-ended class AB transresistance amplifiers like the one of the figure.

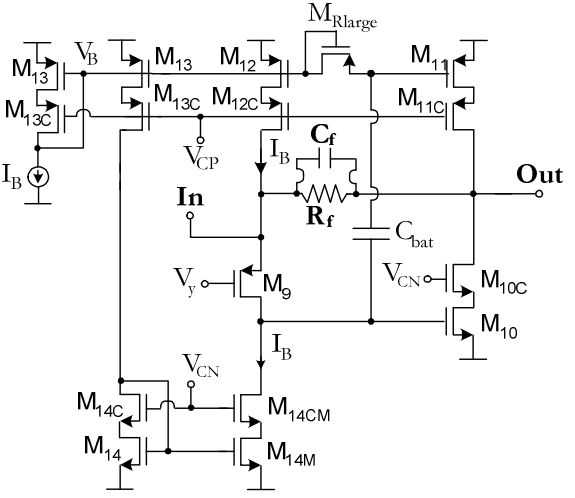

Figure 5.6. Proposed class AB Amplifier

The input current is sensed at the low-impedance input node and driven to resistance R_f, yielding the output voltage. As shown in (5.4), the value of R_f determines the maximum gain of the VGA. Note that the same two-stage amplifier used in the voltage followers of the transconductor (in unity-gain negative feedback in that case) is used for the transresistance amplifier. However, in this case compensation is needed, hence C_f is included. The amplifier input (source of M_9) is a virtual ground with DC voltage V_y+V_{SG9}, where V_y is a bias voltage. This improves linearity of the resistive current division at the transconductor output [16] and allows a stable common-mode voltage at the output of the transconductor and VGA, making the use of a CMFB circuit unnecessary and thus saving power and area.

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By combining Sections 5.2.1.1 and 5.2.1.2, the complete schematic of the VGA is shown in Figure 5.7.

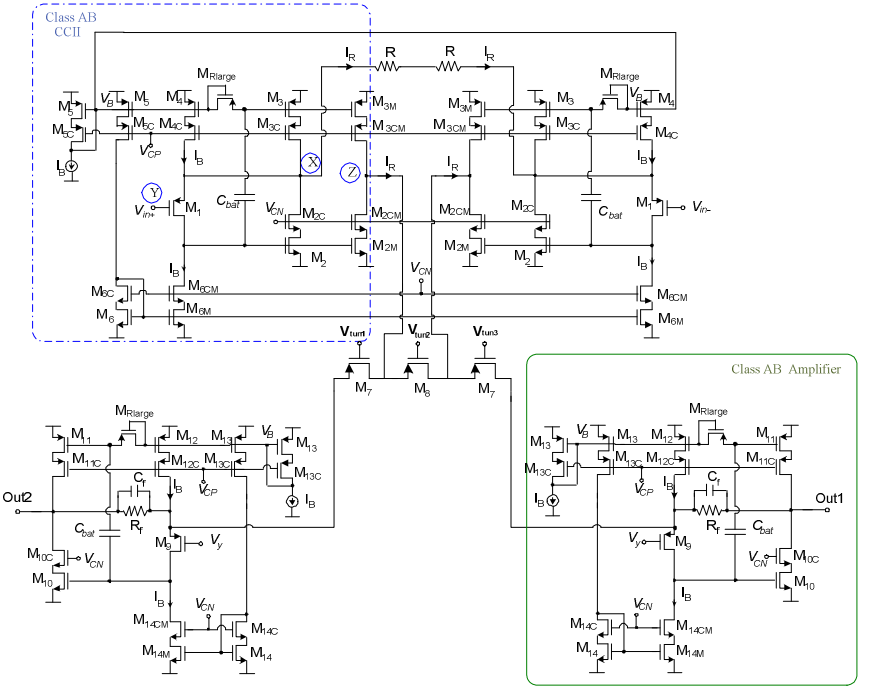

Figure 5.7. Proposed class AB VGA

5.2.2 Bandwidth Invariance with Gain

Figure 5.8 shows the small-signal model of the single-ended version of the VGA in Figure 5.4. Parameters G_m and r_{oT} are the transconductance and output resistance, respectively, of the input transconductor. A single-pole model is used for the output amplifier, whose DC gain, pole frequency and output resistance are A_d, $\omega_p=1/(r_pC_p)$, and r_{oA}, respectively.

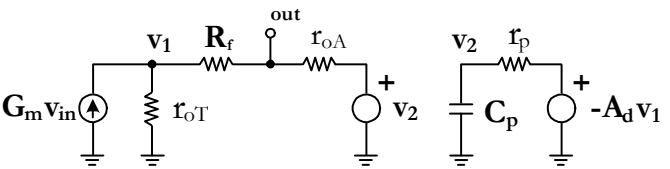

Figure 5.8. Small-signal model of the VGA (single-ended version)

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Routine small-signal analysis shows that the closed-loop gain of the VGA, assuming that $r_{oA}<<R_f$, is

$$A_{CL}(s) \approx G_m R_f \frac{1}{1+\frac{s}{A_d\omega_p}\frac{R_f}{(R_f||r_{oT})}} \qquad (5.5)$$

Therefore, the closed-loop bandwidth is

$$\omega_{CL} = A_d\omega_p \frac{R_f||r_{oT}}{R_f} \qquad (5.6)$$

which assuming that $r_{oT}>>R_f$ simply becomes

$$\omega_{CL} \approx A_d\omega_p \approx GBW \qquad (5.7)$$

Hence, bandwidth is independent of the gain, $A_{CL}=G_mR_f$, and that maximum bandwidth is theoretically achieved. Note from (5.5) that if gain is set by adjusting G_m bandwidth is constant with gain even if the condition $r_{oT}>>R_f$ is not met. This simple analysis does not consider extra poles of the amplifier and transconductor, which may reduce the bandwidth achievable.

5.2.3 Process and Temperature Variations

Process corner simulation, Figure 5.9, shows that for minimum VGA gain, deviation of gain is less than ±0.2dB, and for maximum gain it is ±0.06dB, highlighting the robustness of the design against process variations. The reason is that gain is set by the ratio of passive resistors R and R_f, and the current splitting is set by ratios of active resistors as equation (5.4) reflects.

Simulations in the temperature range [-20ºC, 80ºC] show maximum gain deviations of ±0.12dB and ±0.02dB when the VGA is configured with minimum and maximum gain, respectively. Maximum gain results have been represented as an example in Figure 5.10. This low temperature sensitivity is due to the equal temperature coefficients of resistors R and R_f, cancelling thermal drift in R_f/R, and to the relative insensitivity to temperature variations of current splitting by M_7-M_8.

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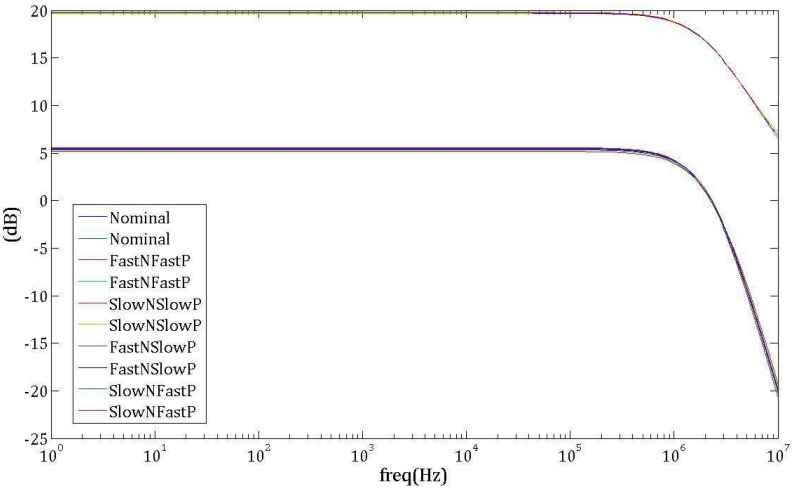

Figure 5.9. Process Corner Simulation

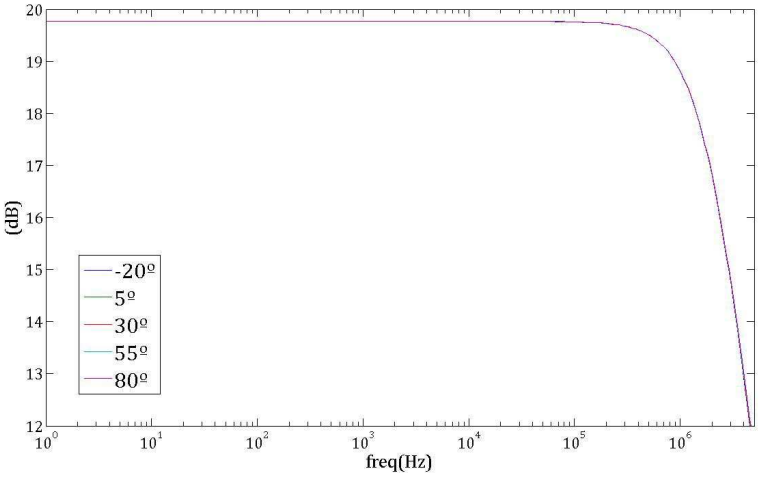

Figure 5.10. Temperature Simulation (maximum gain)

5.2.4 Simulation Results

Before being implemented in a CMOS technology, the VGA has been verified with simulations using Spectre. The circuit has been biased using ±1.65 V power supplies and a bias current of 10 μA. The value of the compensation capacitor C_f is 800 fF. Considering R = 10 kΩ and R_f = 100 kΩ, the maximum gain achievable is 20dB.

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Firstly, Figure 5.11 shows the magnitude frequency responses for different tuning voltages. It can be seen that the bandwidth keeps approximately constant for all the gain values (~1.8 MHz).

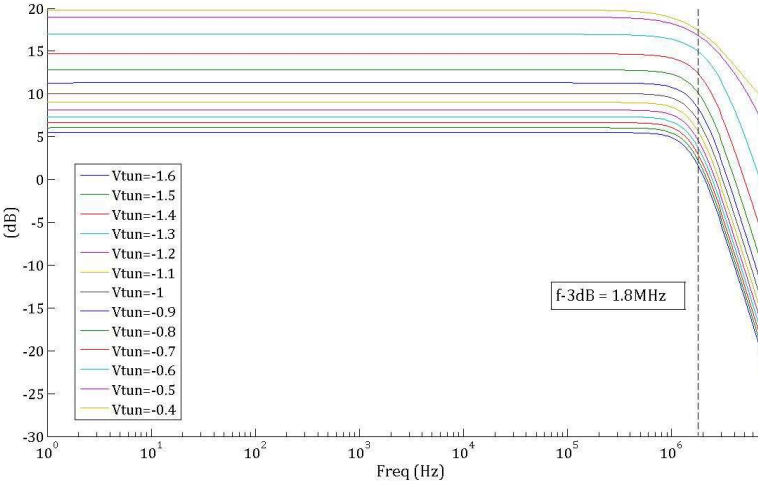

Figure 5.11. Frequency responses for different tuning voltages

In order to verify the settling performance of the VGA when the gain is changed, the transient simulation of Figure 5.12 is performed. A pulse in the tuning voltage is applied so it changes abruptly from -1.2V to -0.7V. It can be clearly seen that the response to the variation made is very fast, without ringing.

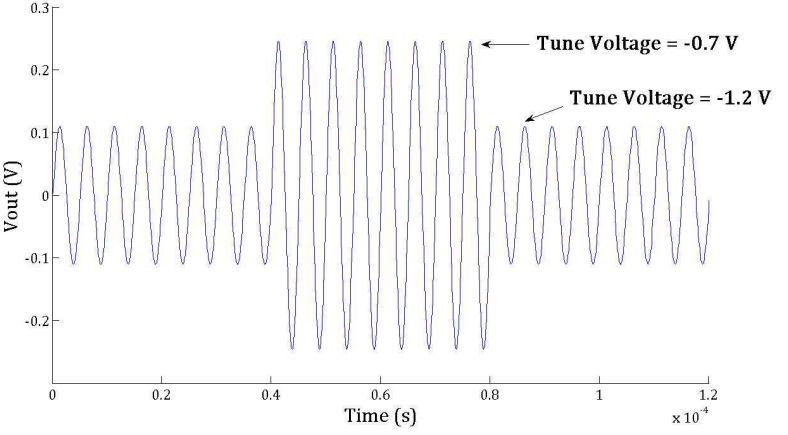

Figure 5.12. Transient simulation: output settling performance when gain is changed

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Linearity of the VGA is shown in Figure 5.13. Harmonic distortion can be seen for the same circuit operating in class A and class AB. Operation in class A is achieved by disconnecting the floating capacitors C_{bat} in the VGA. Second-order harmonic distortion (HD2) curves have not been drawn because their value is lower than -200dB for all the inputs. It must be highlighted that linearity results are much better with class AB operation. In class A configuration, as the input power increases, the degradation is higher than in class AB.

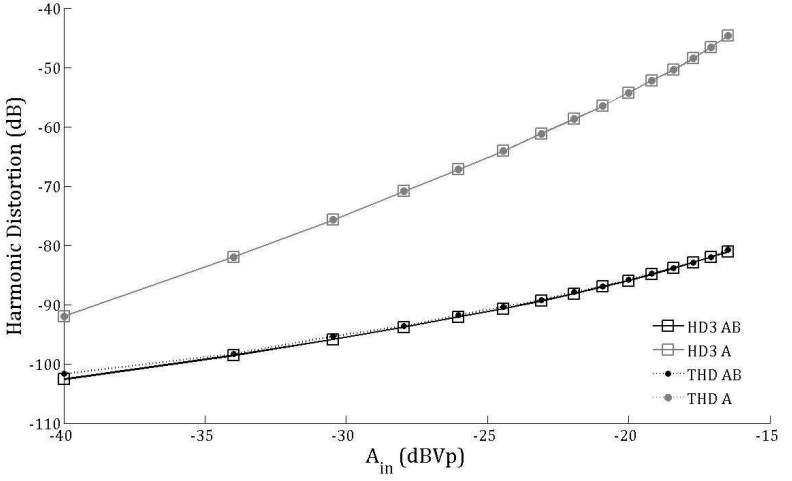

Figure 5.13. Harmonic Distortion

Table 5.1 presents the main parameters and simulation results obtained.

Table 5.1. Simulation Parameters and Results

Parameter	Value
Power Supply	±1.65 V
BW	1.8 MHz
Gain Range	4-20 dB
IM3 @120mVpp, Gmax	-53.4 dB
THD @1MHz, @120mVpp, Gmax	-47.9 dB
IIP3	17.6 dBm
CMRR	145 dB
PSRR+	96 dB
PSRR-	100.7 dB
Eq. input noise	265 nV/√Hz
Power Consumption	500 μW
Die Area	0.25 mm²

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5.2.5 Measurement Results

Once verified, the proposed scheme has been implemented in a standard 0.5μm CMOS n-well process with nominal nMOS and pMOS threshold voltages of 0.64 V and –0.92 V, respectively [17]. As in simulation, the circuit has been biased using ±1.65 V power supplies and a bias current of 10 μA. The bias voltages were generated externally and are V_{CP}= -0.5V, V_{CN}= 0.5V and V_y= -0.3V. The value of the compensation capacitor C_f is 800 fF. The nominal values of the passive resistors are R = 10 kΩ and R_f = 100 kΩ. The dimensions of the transistors employed are listed in Table 5.2 (same dimensions as in simulation).

Table 5.2. Transistor Aspect Ratios

Transistor	Value (μm/ μm)
M_1, M_3, M_{3M}, M_4, M_5, M_{6C}, M_{6CM}, M_9, M_{11}, M_{11M}, M_{12}, M_{13}, M_{14C}, M_{14CM}	100/1
M_2, M_{2M}, M_{10}, M_{10M}	60/1
M_{2C}, M_{2CM}, M_{10C}, M_{10CM}	60/0.6
M_{3C}, M_{3CM}, M_{4C}, M_{5C}, M_{11C}, M_{11CM}, M_{12C}, M_{13C}	200/0.6
M_6, M_{6M}, M_{14}, M_{14M}	100/3
M_7	200/1
M_8	400/1
M_{Rlarge}	1.5/0.6

Figure 5.14 shows the measured magnitude frequency responses for different tuning voltages. Note that the bandwidth keeps approximately constant (1.4MHz) for all the gain values. The measured gain range for V_{tun2} varying from -1.6V to -0.4V (V_{tun1}=-1.65 V) is from 5 to 20 dB. Various VGA stages can be readily cascaded, extending the gain tuning range. The result is quite similar to the one obtained in simulation.

In order to verify the settling performance of the VGA when the gain is changed, Figure 5.15 has been obtained. A step in the tuning voltage is applied so it changes abruptly from -1.2 V to -0.8 V. It can be clearly seen that, as in simulation, the measured response to the variation made is very fast, without ringing.

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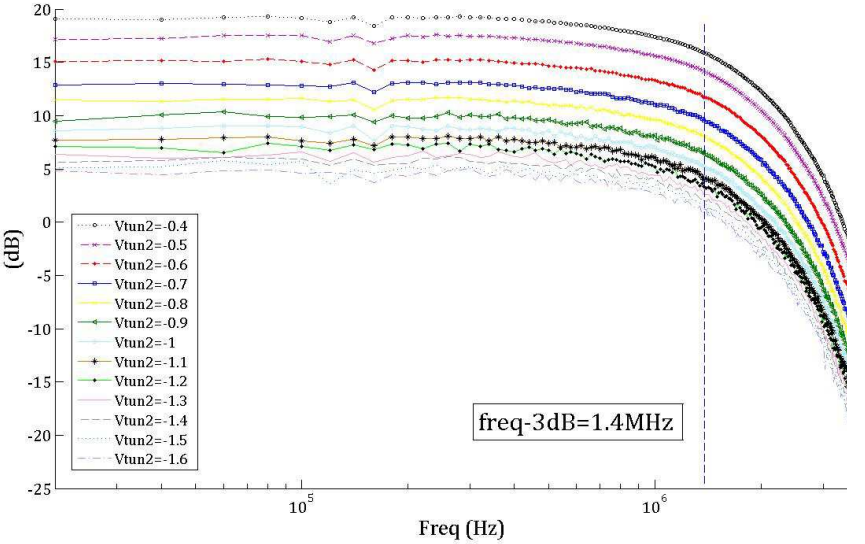

Figure 5.14. Measured frequency responses for different tuning voltages

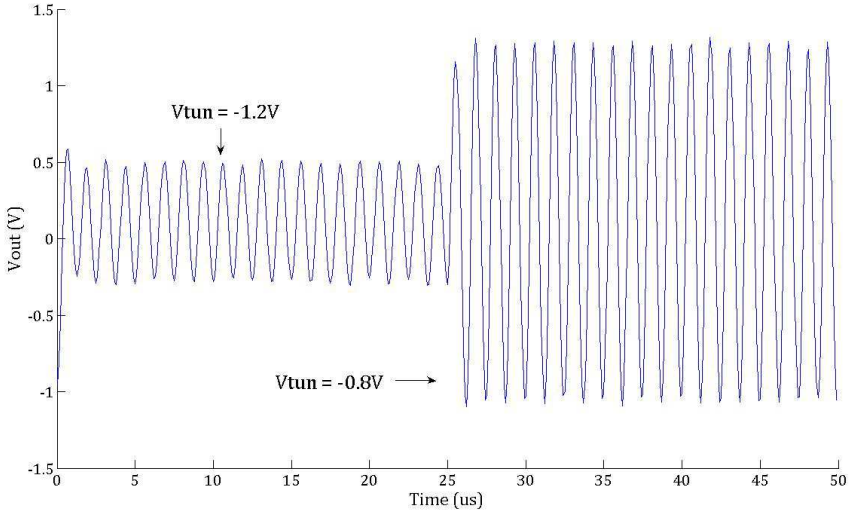

Figure 5.15. Measured output settling performance when gain is changed

Linearity measurements of the VGA are shown in Figure 5.16. Two tones of 350 kHz and 400 kHz have been used. The IIP3 value has been obtained for minimum gain G_{min}. Note that an IIP3 of 13 dBVp has been achieved.

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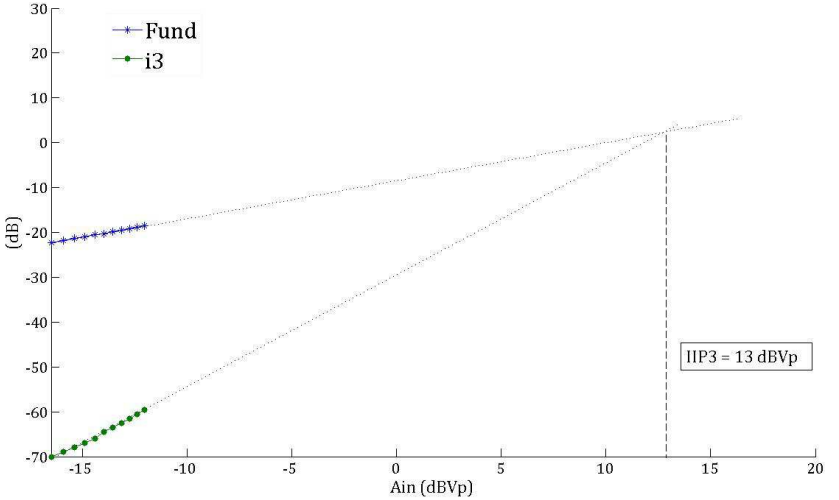

Figure 5.16. Measured IIP3 value obtained with Gmin

Figure 5.17 shows the measured VGA Common-Mode Rejection Ratio (CMRR) versus frequency. Gain of the VGA was set to 20 dB. Note that values above 60 dB are achieved in all the passband of the VGA. A summary of the main measurement results obtained is presented in Table 5.3.

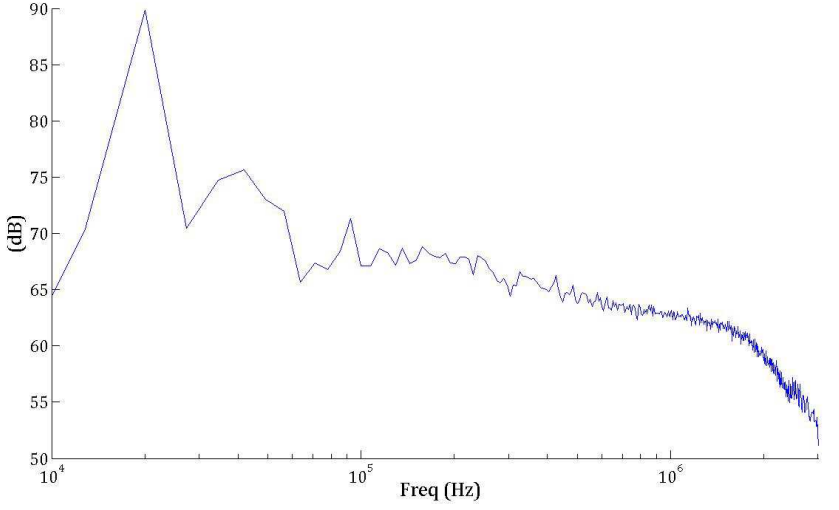

Figure 5.17. Measured CMRR

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Table 5.3. Summary of Measured Performance

Parameter	Value
Power Supply	±1.65 V
BW	1.4 MHz
Gain range	5-20 dB
IM3 @300mVpp each, Gmin	-48 dB
THD @200kHz, @140mVpp, Gmax	-54 dB
In-band IIP3 (Gmin) (Gmax)	13 dBVp 0.5 dBVp
Out-of-band IIP3 (Gmin) (Gmax)	12 dBVp 0 dBVp
CMRR@50kHz,Gmax	75 dB
PSRR+@50kHz,Gmax	71 dB
PSRR- @50kHz,Gmax	60 dB
Eq. input noise @1MHz, Gmax	3 $nV_{rms}/\sqrt{Hz}$
Die area	0.25 mm^2
Power Consumption	500 µW

A microphotograph of the circuit is shown in Figure 5.18. It contains two different versions of the VGA (one of them is inside the white square).

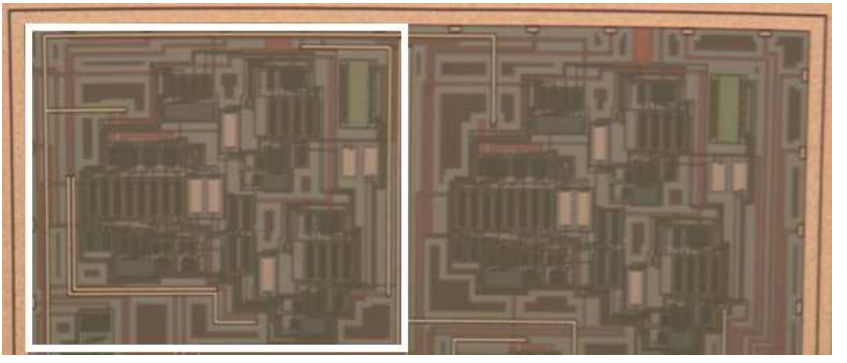

Figure 5.18. Microphotograph of the VGA

Finally, Table 5.4 shows a performance comparison with different reported VGAs [3], [18–22]. Gain tuning range is lower since a single VGA stage has been fabricated, while typically 3 or more stages are used in other works. Note from Table 5.4 that despite the old technology used in this work, our design

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compares favorably in terms of power consumption per stage, providing good performance in terms of linearity and noise.

Table 5.4. Comparison of Measured Performance of Various Reported VGAs

References	**[18]**	**[19]**	**[20]**	**[21]**
CMOS Process	90nm	0.18μm	0.5μm	0.35μm
Bandwidth (MHz)	100	3.84	20	2.87
Number of stages	5	1	5	3
Gain (dB)	13.5~67.5	0~16	0~70	0~60
Power (mW)	13.5 (inc. filter)	1.8	33	11.25
Supply (V)	1.4	1.8	3.3	2.5
VGA area (mm^2)	0.55	N/A	0.24	2.55 (I/Q)
Noise	19 nV/√Hz	4 dB (NF)	9 nV/√Hz	5.2 dB (NF)
IIP3 @Gmin (dBm)	2	3	20	16.2
References	**[22]**	**[3]**	**This work**	
CMOS Process	0.35μm	0.25μm	0.5μm	
Bandwidth (MHz)	246	30-210	1.4	
Number of stages	3	4	1	
Gain (dB)	-15~45	-35~55	5~20	
Power (mW)	27	27	0.5	
Supply (V)	3	2.5	3.3	
VGA area (mm^2)	0.64	0.49	0.25	
Noise	8.7 dB (NF)	8 dB (NF)	3 nV/√Hz	
IIP3 @Gmin (dBm)	-4	7	23 (13 dBVp)	

To sum up, measurement results confirm that the proposed class AB VGA is able to operate with constant bandwidth for all the gain settings, achieving low static power consumption. The cascade connection of transconductor and transresistor is especially adequate for low-power VGA design. As in the filter application, class AB operation is achieved in a simple way using QFG techniques, without increasing power consumption or supply voltage requirements. Among the possible applications of the proposed VGA, AGC circuits in wireless receivers are included.

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5.3 Three-Stage VGA with Offset Control

As in the filter case, some modifications can be done to the circuit in order to improve it. According to the results in Table 5.4, one of the main changes to do is increasing the Gain Tuning Range because, comparing it with other reported VGAs and considering typical receiver specifications, is too low. Consequently, more stages must be added to the original design. Moreover, if more stages are included in the design, an offset control is necessary.

This Section is going to be focused on these improvements. After applying them, several simulations will be done to verify the advantages of the proposed changes.

5.3.1 Three-Stage VGA

First of all, it must be said that before cascading three VGAs to achieve a higher gain and better results, the dimensions of one transistor have been changed in the original one-stage VGA shown in Figure 5.7 in order to improve its performance. By changing the dimensions of just one transistor of that figure, transistor M_8 included in the current-divider (now W/L = 800μ/1μ), the gain tuning range suffers an important increase and, instead of covering gains from 5 to 20dB (Table 5.4), it now contains gains from 0 to 20dBs. This improved one-stage VGA, with the transistor aspect ratios presented in Table 5.2 except M_8 that adopts this new mentioned dimension, is the one that is going to be cascaded to implement the three-stage VGA. Figure 5.19 illustrates this new circuit.

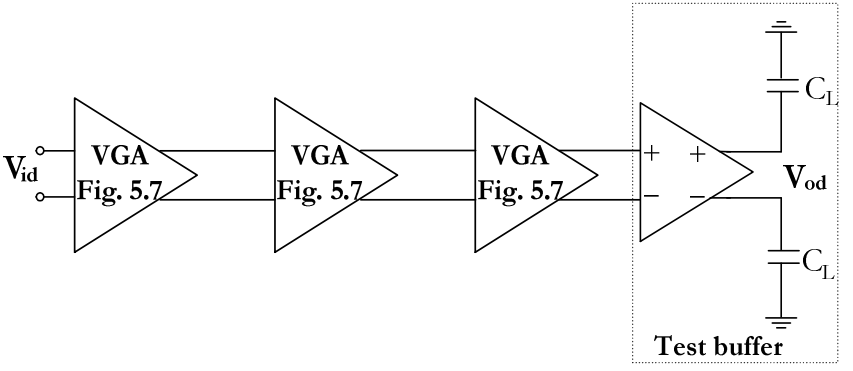

Figure 5.19. Proposed three-stage VGA

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This circuit has been verified with simulations using Spectre. It has been biased using ±1.65 V power supplies and a bias current of 10 μA. The value of the compensation capacitor C_f is 800 fF, and the values of the passive resistors, that define the maximum gain achievable, are R = 10 kΩ and R_f = 100 kΩ.

The first simulation, Figure 5.20, shows the magnitude frequency responses for different tuning voltages. Note that the bandwidth keeps approximately constant (1MHz) for all the gain values. Gain range for V_{tun2} varying from -1.65V to -0.4V goes from 3 to 62 dB, almost 60dBs.

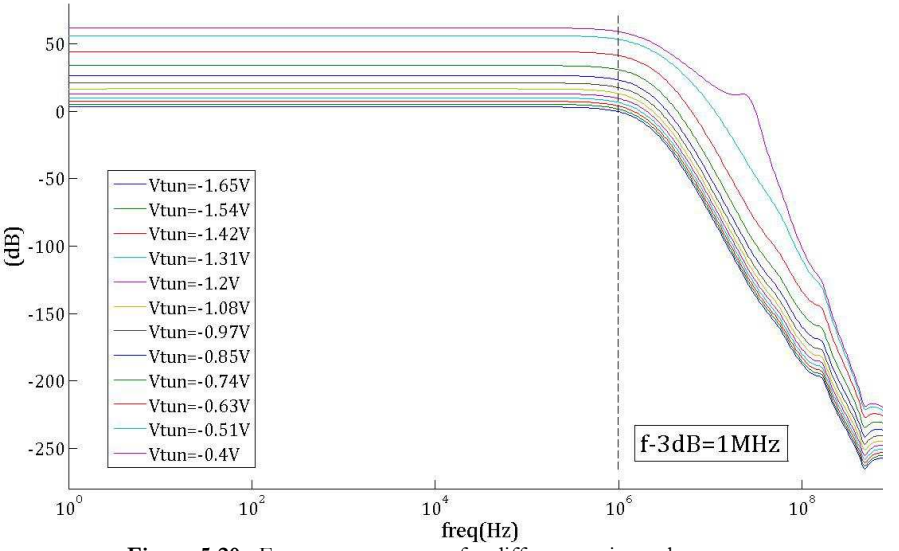

Figure 5.20. Frequency responses for different tuning voltages

Linearity of the VGA is shown in Figure 5.21, where Total Harmonic distortion has been obtained through simulation. It must be highlighted that linearity results are below -50dB for all tuning values.

Table 5.5 presents the main parameters and simulation results obtained for this circuit. Obviously, some of the parameters are better than in the one-stage configuration, like the gain range, while others have clearly worsened, like the noise or the IIP3. Depending on the specific needs of a circuit, more or less stages should be implemented.

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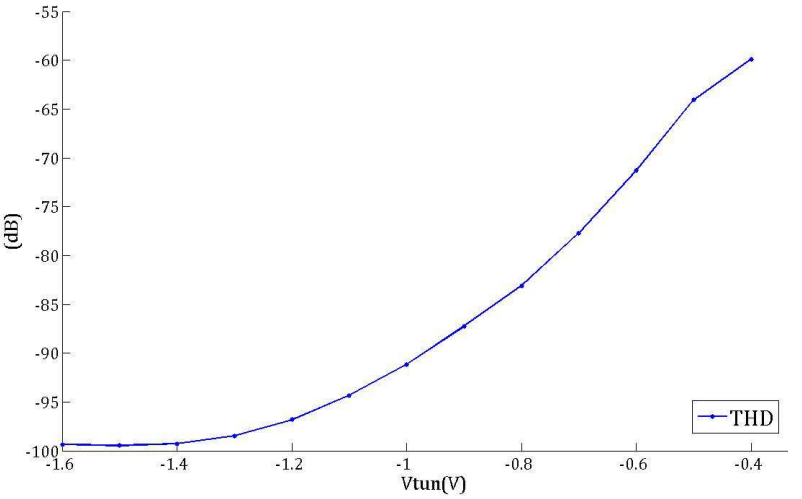

Figure 5.21. Total Harmonic Distortion for different tuning voltages

Table 5.5. Simulation Parameters and Results

Parameter	Value
Power Supply	±1.65 V
BW	1 MHz
Gain range	3-62 dB
THD @200kHz, @1mVpp, Gmax	-60 dB
In-band IIP3 (Gmin) (Gmax)	-14 dBVp -33 dBVp
Out-of-band IIP3 (Gmin) (Gmax)	-8 dBVp -32 dBVp
CMRR@50kHz,Gmax	247 dB
PSRR+@50kHz,Gmax	220 dB
PSRR- @50kHz,Gmax	217 dB
Eq. input noise @1MHz, Gmax	112 $nV_{rms}/\sqrt{Hz}$

5.3.2 Offset Control

As it has been mentioned in previous chapters, DC offset is one of the main drawbacks in zero-IF receivers [23]. Signal is down converted directly to baseband in these receivers, so any kind of offset can worsen it. Moreover, as most of the amplification takes place in the baseband chain as well, the offset is

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amplified too and can even reach levels that saturate the remaining stages [24]. For these two main reasons, DC offset must be eliminated.

Two types of offset errors can be found, the static one or constant in time and the dynamic one or variable in time, and multiple techniques have been employed to eliminate them. Usually, by using AC coupling, low-pass filters or feedback loops, static offset can be eliminated [25–28] while dynamic one cannot. Digital cancellation techniques have also been tried to eliminate both offsets, static and dynamic [29], [30].

The chosen offset-cancellation method, Figure 5.22, is based on measuring the DC offset at the output of any block of the baseband chain, and feeding it back to its input. It is a simple approach, it does not require a lot of area, and it uses QFG techniques to achieve offset cancellation [31]. The DC sensing circuitry is basically a current mirror operational amplifier with a low pass RC filter at the input stage. The RC low pass filter is implemented by a high-resistance active element (R_{LARGE}) and a capacitor (C). The capacitor can be implemented by the parasitic capacitance of the amplifier input transistor, M_n. Depending on the implementation of the baseband block, the output of the DC-offset correction circuit will be in the form of voltage or current.

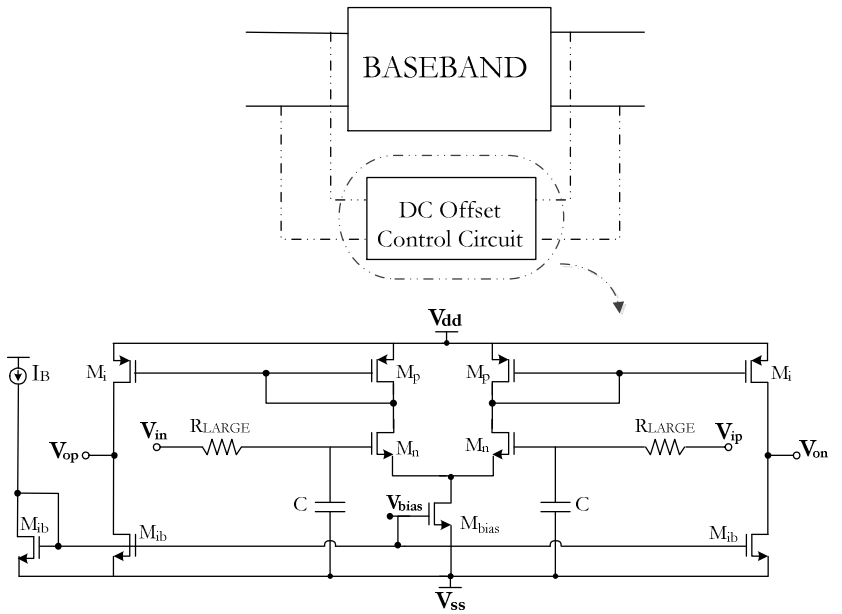

Figure 5.22. Chosen Offset Control Circuit

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The dimensions of the transistors are listed in Table 5.6.

Table 5.6. Transistor Aspect Ratios

Transistor	Value (µm/ µm)
M_p, M_i	288/1.2
M_n	24/1.2
M_{ib}	96/1.2
M_{bias}	192/1.2

The key issue is how to implement a large resistive active element to produce a large time constant, i.e. a low cutoff frequency. Several proposals can be chosen, like the one presented in [31] that uses MOS transistors operating in sub-threshold region to emulate the resistor, achieving GΩ resistances. Another option consists on using the large (and non- linear) leakage resistance of reversed-biased p-n junctions of MOS transistor operating in cutoff region [32], [33]. This simple approach is the one chosen in this work.

However, from one same proposal, several configurations of R_{LARGE} can be implemented [34]. Different topologies are going to be presented in this section, as well as verified through simulations. The complete circuit that is going to be simulated is shown in Figure 5.23, formed by the three-stage VGA proposed previously and one offset cancellation circuit that takes the offset at its output and feeds it back to its input. Different R_{LARGE} implementations allow achieving different DC Offset Control Circuits and different results.

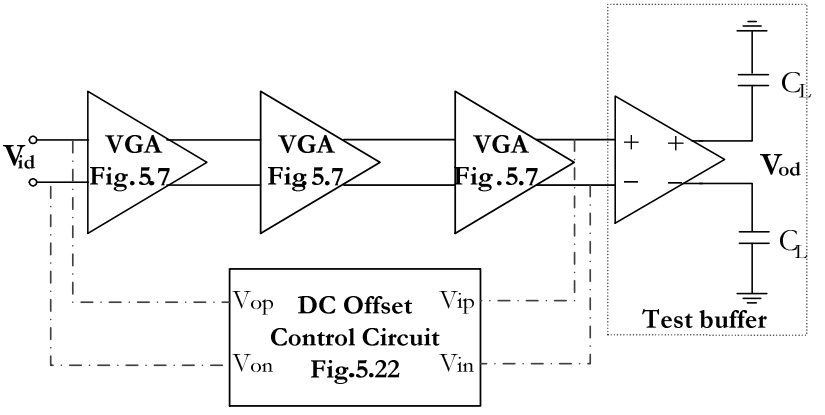

Figure 5.23. Three-stage VGA with Offset Control

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5.3.2.1 R_{LARGE} 1

The first implementation of R_{LARGE} is illustrated in Figure 5.24, where the dimension of both transistors is W = 1.5µm and L = 600nm.

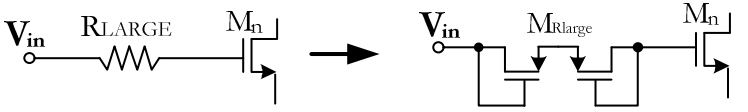

Figure 5.24. R_{LARGE} 1

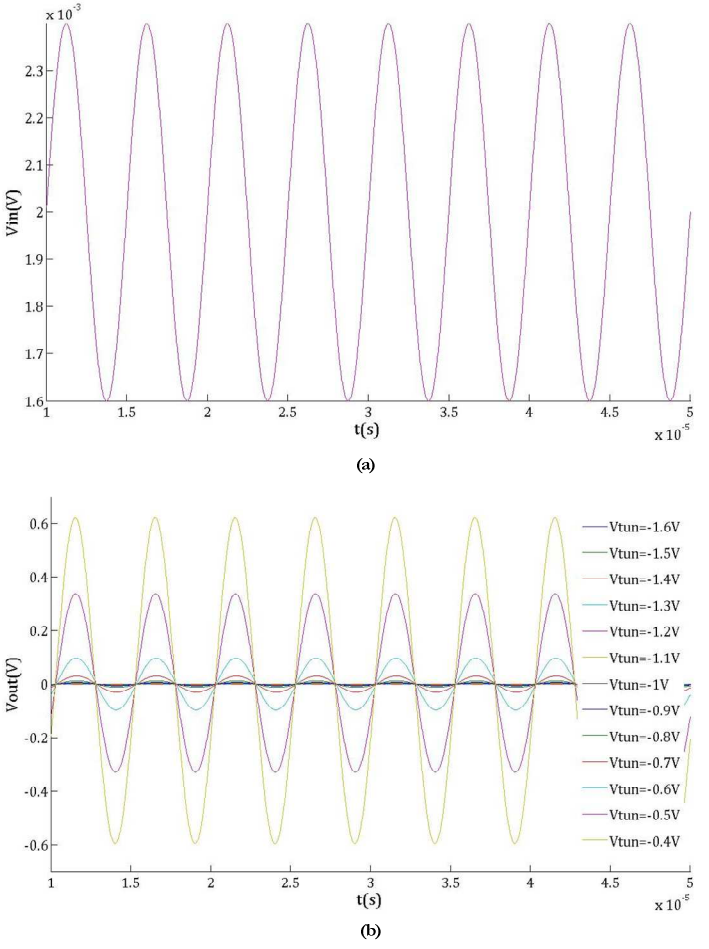

Figure 5.25. (a) Input with offset of 2mV (b) Output for all tuning voltages

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In order to verify the performance of the offset-cancellation circuit, several simulations have been done. Firstly, Figure 5.25 shows the transient results when an input of 800μV_{pp} and 2mV of offset is applied for all the tuning voltages. Low input amplitude has been applied so the output does not present distortion for any gain value. It can be clearly seen that the output has been eliminated.

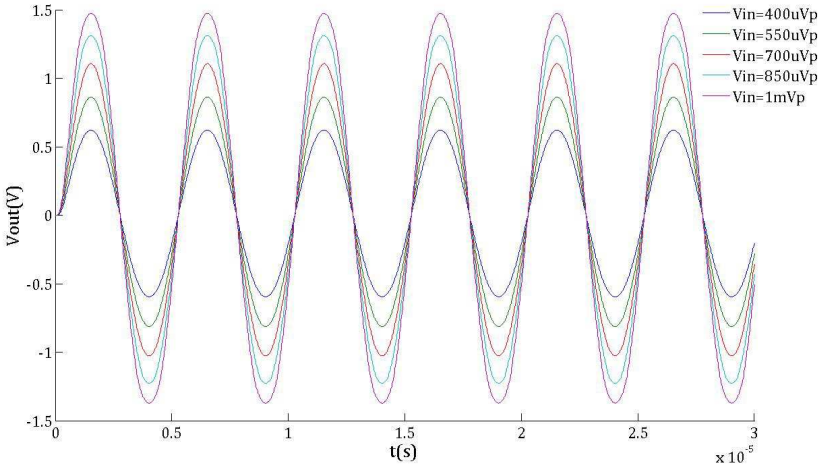

Figure 5.26. Output for different amplitudes (Gmax)

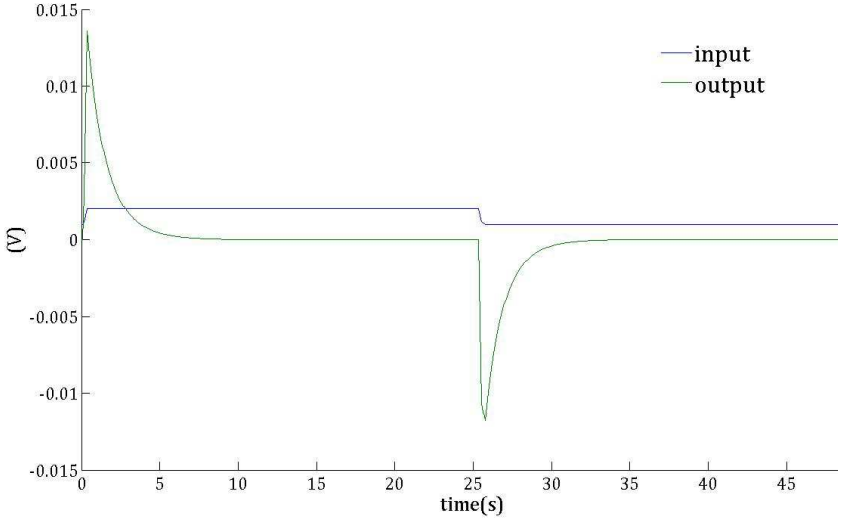

Figure 5.27. Output applying an offset step

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Figure 5.26 shows the transient output when different input amplitudes are applied, with an offset of 2mV for all of them and G_{max} (V_{tun} = -0.4V). Again, offset is cancelled out in all cases.

Lastly, applying a pulse as input, acting as an offset step, Figure 5.27 is obtained. Input changes between 1mV and 2mV, with a delay of 100ms and a period of 50s. Tuning voltage is set to -0.9V. As it can be seen, in spite of the value of the offset at the input, output offset tends to 0.

5.3.2.2 R_{LARGE} 2

Another implementation of R_{LARGE} is illustrated in Figure 5.28, where the dimension of both transistors is again W = 1.5µm and L = 600nm.

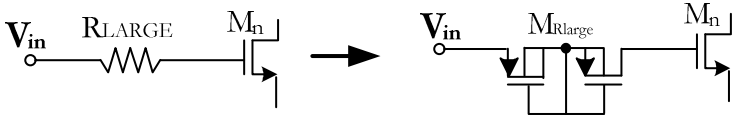

Figure 5.28. R_{LARGE} 2

Doing again the simulations of Section 5.3.2.1, the performance of this new topology is verified. Firstly, Figure 5.29 shows the transient results when an input of 800µVpp and 2mV of offset is applied for all the tuning voltages. Input is not drawn this time because it is already illustrated in Figure 5.25(a).

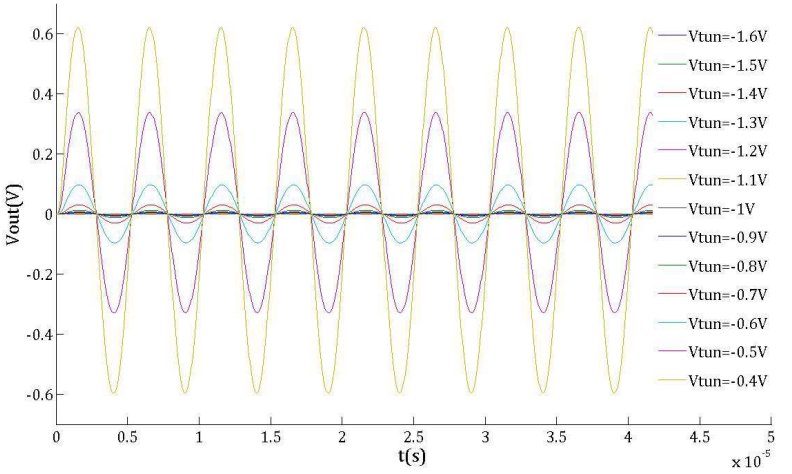

Figure 5.29. Output for all tuning voltages

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For all gain tuning range, the offset applied has been eliminated. Figure 5.30 shows the transient output when different input amplitudes are applied, with an offset of 2mV for all of them and G_{max}. Offset is cancelled out in all cases.

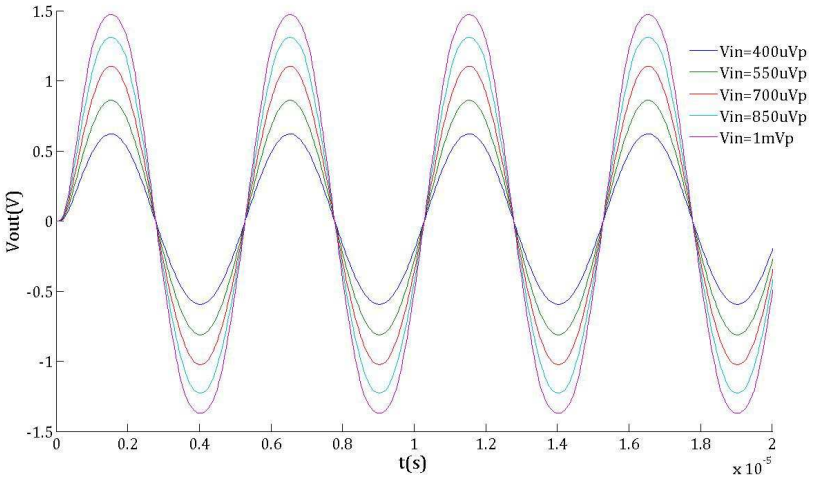

Figure 5.30. Output for different amplitudes (Gmax)

Last simulation, Figure 5.31, applies a pulse as input, acting as an offset step. Input changes between 1mV and 2mV, with a delay of 100ms and a period of 50s. Tuning voltage is set to -0.9V. The output shows that offset tends to 0.

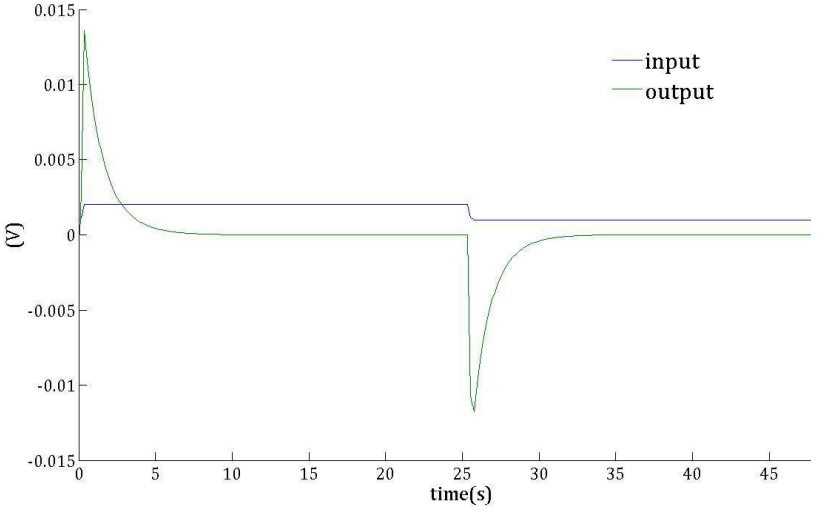

Figure 5.31. Output applying an offset step

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5.3.2.3 R_{LARGE} 3

Figure 5.32 shows the last proposal of R_{LARGE}. The dimension of both transistors is still W = 1.5µm and L = 600nm.

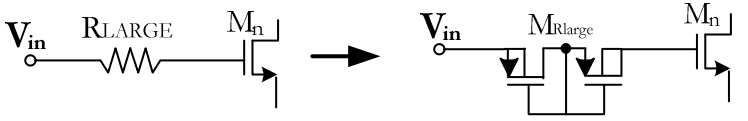

Figure 5.32. R_{LARGE} 3

Once again, Figure 5.33 shows the transient output when an input of 800µVpp and 2mV of offset is applied for all the tuning voltages. Note that offset is eliminated for all tuning voltages, as in previous cases.

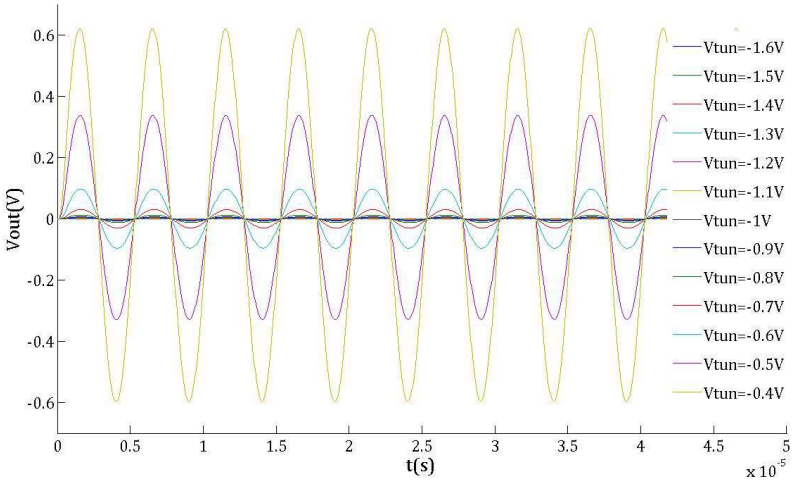

Figure 5.33. Output for all tuning voltages

Figure 5.34, shows the transient output when different input amplitudes are applied, with an offset of 2mV for all of them and Gmax. Offset is cancelled out in all cases.

And finally, Figure 5.35 shows the output when a pulse is applied as input, acting as an offset step. Input changes between 1mV and 2mV, with a delay of 100ms and a period of 50s. Tuning voltage is set to -0.9V. The output shows that offset tends to 0 again.

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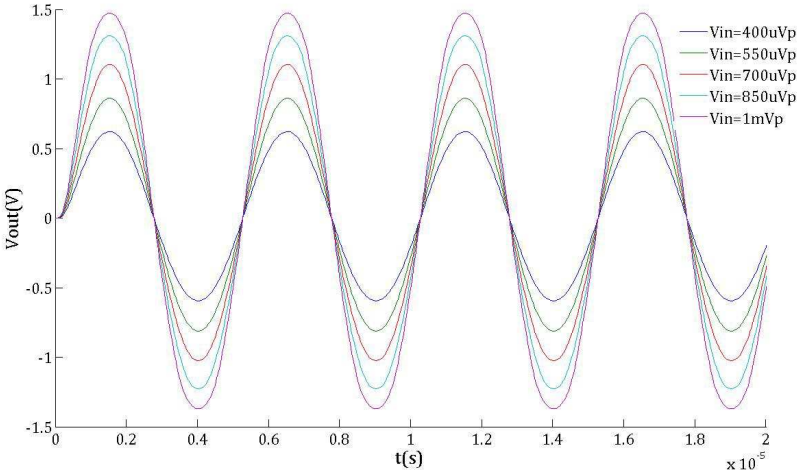

Figure 5.34. Output for different amplitudes (Gmax)

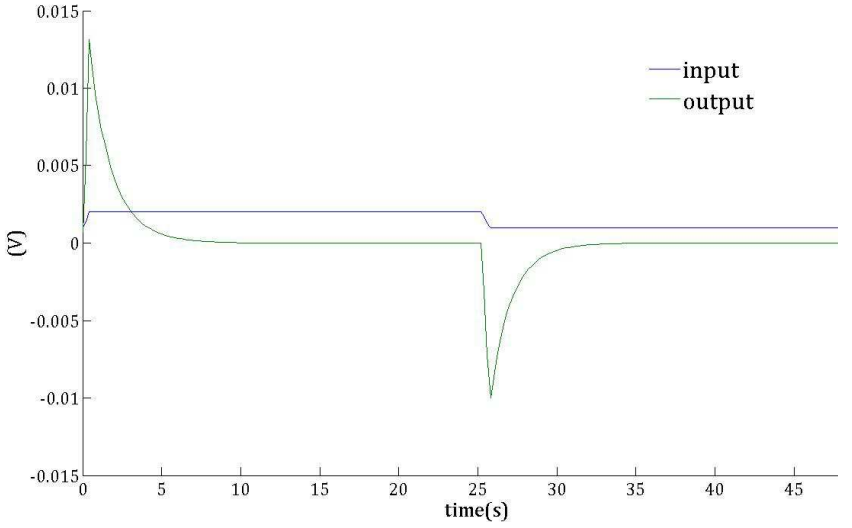

Figure 5.35. Output applying an offset step

There is almost any difference between the implementations of R_{LARGE} studied in this Section. The three of them present similar results. However, small differences can be observed in the "step" figure regarding the peak length or the settling time. The designer should decide which proposal suits the circuit more.

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5.4 Summary

Measurement results confirm that the proposed class AB VGA, presented in Section 5.2, is able to operate with constant bandwidth for all the gain settings, achieving low static power consumption. The cascade connection of transconductor and transresistor is especially adequate for low-power VGA design. Class AB operation is achieved in a simple way using QFG techniques, without increasing power consumption or supply voltage requirements. Applications of the proposed VGA include AGC circuits in wireless receivers.

Section 5.3 has been focused on improving this one-stage VGA by including more stages in the implementation. The more stages it has, the larger its Gain Tuning Range. But, on the other hand, more stages means also that offset affects it more. Consequently, an offset cancellation circuit is needed and has been proposed in this work.

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CHAPTER 6

Conclusions and Future Work

This Chapter summarizes the most significant results and conclusions reported throughout this thesis. The aim of Section 6.1 is to provide a compilation of the main contributions to verify the fulfillment of the objectives proposed in Chapter 1. Furthermore, future research trends related to this work are proposed and briefly analyzed in Section 6.2.

6.1 Conclusions

Almost all the work done in this Ph.D. thesis has been based on applying low-voltage and low-power techniques to analog design -and more specifically to transconductors, G_m-C filters and VGAs design. This was motivated by the proliferation of wireless communication systems and the growing integration factor of electronic circuits, which have been leading to an intensive research in low-voltage low-power techniques, whose application is especially critical in the case of analog circuitry. In the following paragraphs, general conclusions are provided following the structure of this document, i.e. first the proposed new cells are described to end with the design of complete systems.

The state-of-the-art of analog low-voltage low-power design has been summarized in Chapter 1, emphasizing on the advantages involved by using Floating-Gate (FG) and Quasi-Floating-Gate (QFG) techniques, which are the

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basis of most of the circuits proposed in this work. These techniques have been explained in detail in Chapter 2, as well as the applications they are valid for.

Chapter 3 has covered the design technique of high-performance CMOS transconductors, challenging nowadays due to the reduced supply voltages imposed by technology downscaling and low power requirements. Throughout this Chapter, in order to implement a proper transconductor, different circuits intended for its final topology have been proposed, verified and compared, being selected only the better ones. Thanks to them, suitable transconductors for wireless receivers have been implemented by using a systematic approach and the techniques proposed in Chapter 2. This new family of transconductors features high linearity in a wide input range, class AB operation and continuous tuning of their transconductance value.

A complete wide range tunable highly linear third order Butterworth low-pass G_m-C filter has been presented in Chapter 4. After explaining the type of receivers that can make use of it, the filter has been designed block by block. Its basic cell, the class AB programmable transconductor, has been implemented following the techniques explained in Chapter 3. Quasi-floating gate transistors have been used in order to obtain this class AB operation. As a result, the circuit features high current driving capability and, at the same time, very low quiescent power consumption. Besides, each transconductor of the filter includes in its design a technique for tuning the transconductance, chosen among the possibilities presented also in Chapter 3, which allows adjustment of the cutoff frequency. After being implemented, fabricated, measured and analyzed, results lead to affirm that this circuit is useful for channel filtering of highly integrated, low power, multi-standard direct conversion wireless receivers. Furthermore, some improvements to the filter have been done in the second part of the Chapter. Not only its area has been optimized, but also two Automatic Tuning Systems have been proposed, in order to make the filter more practical and better adapted to current necessities.

Finally, in Chapter 5 a Variable Gain Amplifier, another block of vital importance in a Zero-IF wireless receiver, has been proposed, fabricated and measured. Its implementation includes as basic cell again the class AB transconductor designed in previous chapters, so it achieves class AB operation as well thanks to QFG techniques, without increasing power consumption or supply voltage requirements. Moreover, this experimentally validated circuit is able to operate with constant bandwidth for all the gain settings. Also in this Chapter, a three-stage VGA has been proposed, formed by cascading three one-stage VGAs.

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This new class AB VGA achieves larger Gain Tuning Range than the basic circuit, but is also more affected by the offset. Consequently, an offset-cancellation circuit has been added to the implementation, and simulations have been made to verify the usefulness of the circuit.

6.2 Future Work

The work performed in this thesis leads to some future research lines, both concerning basic cell design and system level. The new possible lines of work are specified below.

At cell level:

❖ At this level, the key issue lies in studying the possibilities of the proposed class AB transconductors in other analog systems, not just filters or VGAs. A possible system where this cell could be interesting is an Analog- to-Digital Converter (ADCs), useful for many applications. For instance, continuous-time sigma-delta modulators could benefit from the advantages of these transconductors.

❖ Beside new applications for the transconductors, other possibilities for the SSF cell can be explored as well. This cell has ended up being really versatile in low-voltage analog design since it allows transforming any class A circuit based on it into its class AB version. Consequently, quiescent power consumption is reduced considerably with almost any penalization. Although, throughout this work, this cell has been applied in some designs, many more circuits could enjoy its advantages.

At system level:

❖ Obviously, the most immediate task to do at system level consists in measuring experimentally the chip that contains the optimized filter and the two automatic tuning systems. As it had been fabricated recently, the prototype did not arrive until this thesis was almost finished, so there was not time to measure it

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and include the results in the work. It is necessary since its performance needs to be verified and compared with the obtained simulation results.

❖ Fabricate the three-stage VGA with offset cancellation is another thing that needs to be done. This circuit has already been proposed, implemented and simulated, and satisfactory results have been obtained. In fact, these simulation results suit better the necessities of current receivers than the ones achieved with the one-stage version, and hopefully the experimental ones would do it also.

❖ A different line of work that can be followed is based on implementing the proposed designs in modern deep submicron CMOS processes (e.g. 90nm) to validate their robustness with technology scaling and short-channel effects. This would allow reducing notably the power supply needed and, therefore, the power consumption.

❖ An interesting idea would be to redesign the channel-selection filter proposed for other target applications which require high linearity and could benefit from the active component reduction achieved. For instance, 802.11a/b/g/n WLAN receivers could perfectly make use of it after being redesigned.

❖ Besides the proposals suggested in relation to the specific circuits developed in this thesis, there are other possible future lines of work related to other aspects. An idea would be studying new filtering topologies, more efficient regarding power consumption. One possibility would consist in studying filters formed by transconductors with multiple and complementary outputs, since that would allow recovering the current lost in the attenuation phase (current divider).

❖ Finally, in order to have a complete baseband chain of the receiver, an Automatic Gain Control (AGC) needs to be implemented. Besides the proposed VGA with offset-cancellation, which constitutes the main part of an AGC, a Received Signal Strength Indicator (RSSI) is also necessary to measure the power

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present in a received signal. It could benefit from the implementation of the peak detectors and squarers presented in Chapter 4.

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CHAPTER 7

Conclusiones y Líneas Futuras

En este capítulo se repasan los resultados y conclusiones más significativos obtenidos a lo largo de esta tesis. El objetivo del apartado 7.1 es realizar un resumen de las principales contribuciones del trabajo, corroborando así el cumplimiento de los objetivos propuestos en el Capítulo 1. Además, en el apartado 7.2, se proponen una serie de líneas de trabajo futuras relacionadas con este trabajo.

7.1 Conclusiones

Prácticamente todo el trabajo realizado a lo largo de esta tesis se ha basado en aplicar técnicas de baja tensión y bajo consumo al diseño de circuitos analógicos, y más específicamente al diseño de transconductores, filtros G_m-C y VGAs. El interés en las técnicas de diseño de baja tensión y bajo consumo está suscitado por la proliferación de sistemas de comunicación inalámbricos y el creciente factor de integración de los circuitos electrónicos. La aplicación de estas técnicas es especialmente delicada en el caso de los circuitos analógicos. En los siguientes párrafos, se realiza un recorrido a lo largo del trabajo realizado estableciendo algunas conclusiones generales.

El Capítulo 1 hace un repaso de la situación actual del diseño de circuitos analógicos de baja tensión y bajo consumo, haciendo especial hincapié en las ventajas que aporta el uso de técnicas de puerta flotante (FG: Floating-

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Gate) y puerta cuasi-flotante (QFG: Quasi-Floating Gate), que constituyen la base de la mayoría de los circuitos propuestos a lo largo de esta tesis. Estas técnicas se explican detalladamente en el Capítulo 2, así como las aplicaciones para las que resultan útiles.

En el Capítulo 3 se ha presentado una técnica de diseño de transconductores CMOS de altas prestaciones. Esto supone un reto hoy en día debido a que la reducción de tamaño que están sufriendo las tecnologías, así como los exigentes requisitos de bajo consumo, han provocado una disminución de las tensiones de alimentación. A lo largo de este capítulo se han propuesto, verificado y comparado diferentes circuitos, a fin de seleccionar únicamente los más adecuados para formar parte de la topología final del transconductor. De esta manera, mediante un enfoque sistemático de diseño, los circuitos seleccionados, y las técnicas propuestas en el Capítulo 2, se han implementado transconductores adecuados para receptores inalámbricos. Esta nueva familia de transconductores presenta una gran linealidad en un amplio rango de entrada, operación en clase AB y sintonía continua de su valor de transconductancia.

En el Capítulo 4 se ha presentado un filtro Butterworth Gm-C paso bajo sintonizable de 3º orden altamente lineal. Tras hacer un repaso de los distintos tipos de receptores que podrían utilizarlo, se ha llevado a cabo el diseño del filtro bloque a bloque. Su celda básica, el transconductor clase AB sintonizable, se ha implementado siguiendo las técnicas descritas en el Capítulo 3. La operación en clase AB se ha conseguido gracias al empleo de transistores QFG. A causa de ello el circuito presenta grandes corrientes de salida y, al mismo tiempo, un muy bajo consumo estático. Además, cada transconductor incluye en su diseño una técnica para sintonizar su transconductancia de entre las propuestas en el capítulo anterior, permitiendo así realizar un ajuste preciso de la frecuencia de corte. Los resultados de medida del filtro, una vez fabricado, confirman que el circuito puede emplearse para filtrado de canal en un receptor Bluetooth altamente-integrado de conversión directa. En la segunda parte del capítulo se han realizado algunas mejoras al filtro. En primer lugar, su área se ha optimizado. Y, en segundo lugar, se han propuesto dos sistemas de sintonía automática, cuyo objetivo es adaptar mejor el filtro a las necesidades actuales y hacerlo más práctico.

Por último, en el Capítulo 5 se ha propuesto, fabricado y medido un Amplificador de Ganancia Variable (VGA). Este circuito también constituye un bloque de vital importancia en un receptor de conversión directa. Dado que el transconductor clase AB diseñado previamente es de nuevo la celda básica de su

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topología, este circuito consigue operar en clase AB mediante el empleo de las técnicas QFG y sin necesidad de aumentar el consumo o la tensión de alimentación. Además, el VGA presenta un ancho de banda constante para todas las ganancias de su rango. En este capítulo se ha propuesto también un VGA de tres etapas, cuyo diseño se basa en colocar tres VGAs de una etapa en cascada. Este nuevo circuito alcanza mayores rangos de sintonía de ganancia que el circuito básico de una etapa, aunque se ve mucho más afectado por el offset. A consecuencia de ello, se ha añadido un circuito de cancelación de offset a la implementación del circuito, y se han realizado simulaciones para comprobar el correcto funcionamiento del conjunto.

7.2 Líneas Futuras

El trabajo realizado a lo largo de esta tesis da pie a una serie de líneas de investigación futuras, relacionadas tanto con el diseño a nivel de celda como a nivel de sistema. Específicamente, las posibles nuevas líneas de trabajo son:

A nivel de celda:

❖ A este nivel, la tarea fundamental consiste en estudiar las posibilidades que ofrece el uso del transconductor clase AB en otros sistemas analógicos, no sólo en filtros o VGAs. Un posible sistema dónde esta celda podría resultar interesante es un Convertidor Analógico-Digital (ADC), muy utilizado en diferentes aplicaciones. Por ejemplo, un modulador sigma-delta tiempo-continuo podría beneficiarse de las ventajas de estos transconductores.

❖ Además de nuevas aplicaciones para los transconductores, también se podrían explorar nuevas posibilidades para la celda Super-Seguidor de Fuente (SSF). Esta celda ha resultado ser muy versátil en el diseño analógico de baja tensión, ya que permite transformar cualquier circuito en clase A que la contenga en su correspondiente versión en clase AB. Esto permite reducir considerablemente el consumo estático de potencia sin prácticamente ninguna penalización. A pesar de que, a lo largo de esta tesis, esta celda se ha utilizado en varios diseños, muchos más circuitos podrían disfrutar de sus ventajas.

A nivel de sistema:

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❖ Obviamente, la tarea más inmediata a nivel de sistema consiste en medir experimentalmente el chip que contiene el filtro optimizado y los dos circuitos de sintonía automática. Como ha sido fabricado recientemente, el prototipo no llegó con tiempo suficiente como para incluir los resultados de medida en la tesis. Para poder comprobar si los resultados experimentales coinciden con los de simulación, esta tarea es prioritaria.

❖ Otra línea futura importante consiste en fabricar el VGA de tres etapas con cancelación de offset. Este circuito ya ha sido implementado y simulado, y se han obtenido resultados satisfactorios. De hecho, sus resultados de simulación se adaptan mejor a las necesidades de los receptores actuales que los obtenidos con la versión de una etapa, y cabe esperar que con los resultados experimentales ocurra lo mismo.

❖ Una línea de trabajo diferente consistiría en implementar en tecnologías CMOS submicrométricas (e.g. 90nm) los diseños propuestos en este trabajo, para corroborar su robustez frente al aumento del factor de escala y los efectos de canal corto. Esto permitiría reducir considerablemente la tensión de alimentación necesaria y, por tanto, el consumo de potencia.

❖ Una idea interesante consistiría en rediseñar el filtro de selección de canal propuesto para otras aplicaciones que requieran alta linealidad y puedan beneficiarse de la reducción del número de elementos activos, como por ejemplo los receptores WLAN 802.11a/b/g/n.

❖ Además de las sugerencias relacionadas con los circuitos específicos desarrollados en esta tesis, existen otras posibles líneas futuras. Una idea podría ser estudiar nuevas topologías de filtrado, más eficientes en relación con el consumo de potencia. Una posibilidad consistiría en estudiar filtros formados por transconductores con salidas multiples y complementarias, ya que de esta manera

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se podría recuperar la corriente que se ha perdido en la fase de atenuación (divisor resistivo).

❖ Finalmente, se podría implementar un Control Automático de Ganancia (AGC) para poder disponer de una cadena banda base completa de receptor. Para ello, además del VGA con cancelación de offset que ha sido propuesto y que constituye el bloque principal de un AGC, haría falta también un RSSI (Indicador de fuerza de señal de recepción) que permita medir la potencia de la señal recibida. Para desarrollar este bloque, el diseñador podría beneficiarse de la implementación de los detectores de pico y los elevadores al cuadrado propuesta en el Capítulo 4.

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List of Publications

International Journals

1. A. J. Lopez-Martin, L. Acosta, C. Garcia-Alberdi, R. G. Carvajal, and J. Ramirez-Angulo, "Power-efficient analog design based on the class AB super source follower," *International Journal of Circuit Theory and Applications*, vol. 40, no. 11, pp. 1143–1163, 2012.

2. A. J. Lopez-Martin, J. M. Algueta, C. Garcia-Alberdi, L. Acosta, R. G. Carvajal, and J. Ramirez-Angulo, "Design of micropower class AB transconductors : A systematic approach," Microelectronics Journal, pp. 1–10, 2012.

3. C. Garcia-Alberdi, A. J. Lopez-Martin, L. Acosta, R. G. Carvajal, and J. Ramirez-Angulo, "Tunable Class AB CMOS Gm-C Filter Based on Quasi-Floating Gate Techniques," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1300–1309, 2013.

4. C. Garcia-Alberdi, J. Aguado-Ruiz, A. J. Lopez-Martin, and J. Ramirez-Angulo, "Micropower Class-AB VGA With Gain-Independent Bandwidth," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 7, pp. 397–401, 2013.

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International Conferences

1. C. Garcia-Alberdi, L. Acosta, A. J. Lopez-Martin, J. Ramirez-Angulo and R. G. Carvajal, "Tunable Class AB CMOS Gm-C Channel Filter for a Bluetooth Zero-IF Receiver," XXIV Conference on Design of Circuits and Integrated Systems (DCIS), 2009.

2. C. Garcia-Alberdi, A. J. Lopez-Martin, L. Acosta, R. G. Carvajal, and J. Ramirez-Angulo, "Class AB CMOS Tunable Transconductor," 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2010.

3. A. J. Lopez-Martin, J. M. Algueta, C. Garcia-Alberdi, L. Acosta, J. Ramirez-Angulo and R. G. Carvajal, "A New Family of Micropower Class AB Quasi-Floating Gate Transconductors" XXVI Conference on Design of Circuits and Integrated Systems (DCIS), 2011.

4. C. Garcia-Alberdi, J. Aguado-Ruiz, and A. J. Lopez-Martin, "Power-Efficient Class AB VGA with Gain-Independent Bandwidth," XXVI Conference on Design of Circuits and Integrated Systems (DCIS), 2011.

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